HIGH EFFICIENCY INDUSTRIAL SCREEN PRINTED N-TYPE MC-SI SOLAR CELLS WITH FRONT BORON EMITTER

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ABSTRACT: We have developed a process to fabricate n-type solar cells on large area (156.25 cm^2) multicrystalline substrates involving simultaneous diffusion of phosphorous back surface field and boron emitter, screen-printed metallization and firing through SiN_x, which leads to a record high efficiency of 16.4%. We apply a simple and cost-effective method to passivate industrially produced boron-doped emitters for n-type solar cells with a demonstrated efficiency enhancement of more than 2% absolute. Moreover, it is experimentally demonstrated that the optimum base resistivity for n-type multicrystalline silicon wafers lies between 1.5 to 4 Ωcm. This is a significant step forward for industrial production of solar cells based on n-type mc-Si.
Keywords: Silicon solar cells, n-type, Multicrystalline, boron emitter.

1 INTRODUCTION

N-type silicon has been proven to have a higher tolerance to common transition metal impurities, such as those present in silicon produced from quartz and carbon (such as metallurgical routes), potentially resulting in higher minority carrier diffusion lengths compared to p-type substrates [1,2]. In spite of these advantages, at present, more than 85% of the silicon solar cells produced by the industry are based on p-type substrates. This is caused mostly by an insufficient development and industry implementation of the n-type cell processes based on multicrystalline substrates, which is in turn for a large part due to a poor development of an industrial low-cost technique for passivation of p^+ emitters.

This paper presents solar cell development on n-type multicrystalline substrates with boron front emitter fabricated using low cost processes for industrial use (such as screen printing techniques and microwave Plasma Enhanced Chemical Vapour Deposition (PECVD) of silicon nitride (SiN_x)). We show that good passivation of p^+ emitters can be achieved on highly doped boron emitter (60 Ω/square). Moreover, it is experimentally demonstrated that the optimum base resistivity for n-type multicrystalline silicon wafers lies between 1.5 to 4 Ωcm.

2 RESULTS AND DISCUSSION

2.1 Passivation of boron emitters

One of the major development areas of the n-type mc-Si solar cell process remains the passivation of the front side boron emitter. Since the conventional way to passivate n^+ emitters, for the p-type solar cell process, using a PECVD-SiN_x layer results in a poor or no passivation for p^+ emitters, a new way of passivating p^+ surfaces needs to be developed [3,4]. A way to solve this issue is by using an intermediate SiO_2 layer between the SiN_x and the Si wafer, or even by using SiC_x as a passivation layer [3-6]. However, the SiO_2 layer is thermally grown at high temperature for a long time, which could result in degradation of mc-Si wafer and an increase in production cost of the cells and is also a batch-like process. We have developed a new method to passivate p^+ emitters which brought new potential of the n-type multicrystalline industrial solar cell process. This method relies on the same PECVD SiN_x technology as is widely used in industry to passivate n^+ (phosphorous) emitters, which is industrially applicable with no substantial increase in cost or process time.

In order to investigate this new passivation method on p^+ emitters, we have fabricated symmetric $p^+/n/p^+$ devices and measured the lifetime of minority charge carriers using Quasi Steady-State PhotoConductance (QSSPC) setup. This device structure is widely used in literature in order to study the surface passivation or the emitter quality of a cell process [3-5]. Precisely these devices were fabricated on polished n-type FZ-Si substrates with resistivity of 3.8 Ωcm followed by boron emitter diffusion (80 Ω/square) on both sides (at University of Konstanz) and a subsequent glass removal and cleaning of the surfaces (at ECN). On the clean surfaces the new passivation has been applied which we denote as «improved SiN_x» passivation. For comparison we also fabricated reference devices on which the standard SiN_x layer was used as a passivation method. In table I the resulting effective lifetime and implied V_{oc} values of the best devices are shown after a firing step for both passivation methods. It should be noted that firing at a high peak temperature is necessary in an industrial process to be able to make Ohmic contact between printed metal fingers and Si. Therefore the meaningful values for the effective lifetime and the implied V_{oc} are only after a firing step at similar temperatures as are used for the solar cell process.

Table I: Minority carrier lifetime (τ_{eff}) and implied V_{oc} from measurements on symmetric $p^+/n/p^+$ devices using QSSPC at an injection level of 1×10^{15} cm^{-3} (after firing).

Passivation method	τ_{eff} [µs]	Implied V_{oc} [mV]
standard SiN_x	100	600
improved SiN_x	588	660

Almost 6-fold enhancement in the lifetime and 60 mV higher implied V_{oc} is observed for devices passivated by the «improved SiN_x» method. These values outperform even the results obtained using thermal SiO_2/SiN_x stacked layers as a passivation method [3,4].

The enhanced minority carrier lifetime observed

when the p^+ surface is passivated by the «improved SiN_x» method is expected to be visible also in the solar cell results. For this purpose, test solar cells have been fabricated using an inline n-type cell process. Table II shows the parameters measured on solar cells fabricated (see table caption) using neighbouring wafers in which the surfaces are passivated by both methods presented above. Since cell processes are otherwise exactly the same, and the wafers are neighbours, the difference in conversion efficiency must come from the passivation method used. The results clearly indicate that an enhancement in solar cell efficiency of about 2% absolute is achieved using the newly developed passivation method as compared with the standard SiN_x passivation method industrially used for phosphorous emitter passivation.

Table II: Comparison of the mc-Si solar cell parameters. The solar cells were fabricated on isotexture etched n-type mc-Si wafers (0.56 Ωcm, with area of 100 cm^2), having boron (60 Ω/square emitter) and phosphorous (BSF) diffusion done in the belt furnace, and standard screen printing metallization. The wafers under test are neighbours in the ingot.

Passivation method	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	η [%]
standard SiN_x	27.0	567	73.8	11.3
improved SiN_x	30.3	591	74.5	13.3

In order to explain this huge enhancement in power conversion efficiency when the p^+ emitter is passivated using the new method, the internal quantum efficiencies (IQE) for standard SiN_x passivation and «improved SiN_x» passivation were compared. It is clear from figure 1 that the «improved SiN_x» passivation has a profound effect on boron emitter passivation since the IQE is strongly enhanced for wavelengths below 700 nm. Consequently, the V_{oc} and J_{sc} of the cell are increased, as can be seen in table II. On the other hand, the rear side IQE is very low and is strongly influenced by the wafer base resistivity, indicating the importance of the Back Surface Field (BSF). However, for the wafers with the same resistivity (as those presented in the figure) the effect of the «improved SiN_x» passivation on rear side IQE (phosphorous BSF) is clearly visible.

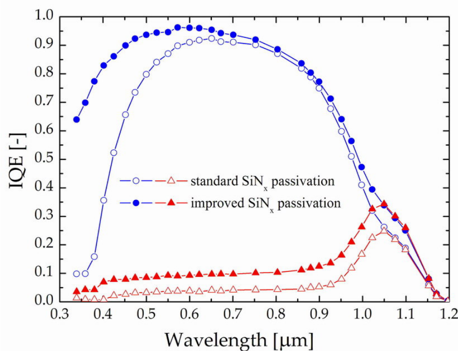

Figure 1: Internal quantum efficiency of the solar cells measured by illuminating the front side (circles) and rear side (triangles), for both passivation methods (see legend). The wafers tested are neighbours and have a base resistivity of 0.56 Ωcm.

2.2 Inline versus batch process for boron diffusion

In order to further develop our n-type cell process it is important to know the most promising process to obtain maximum efficiency gain versus cost. Due to asymmetric capture cross section of the recombination centres of many transition metal impurities in multicrystalline silicon, n-type doped substrates are expected to be more favourable in this respect than a p-type doped substrate [1,2]. However, in order to realize an emitter on the n-type Si substrate, a p^+ diffusion (usually boron) should be performed. The diffusion of boron requires a temperature higher than 900ºC and boron does not have such a significant gettering effect as phosphorus [8,9]. Therefore, sources of contamination should be kept away more carefully than in the case of phosphorus (n^+) diffusion [10].

Here we have made a comparison of two diffusion processes for boron emitters: an inline process, where the emitter diffusion is carried out in an infrared conveyor belt furnace, and a batch process where diffusion is conducted in a horizontal quartz tube furnace with an industry-compatible scale (maximum load of 400 wafers of 15.6×15.6 cm^2). Several different boron sources were investigated, such as a commercial boron paste (for screen-printing), a comercial boron liquid (for spin-on), and a boron tribromide (BBr_3) liquid bubbled by N_2 (for tube furnace diffusion). Similar to the previous section, the investigation was first focused on comparison of lifetime and implied V_{oc} of symmetric $p^+/n/p^+$ devices fabricated on polished n-type FZ-Si wafers with base resistivity of 3.8 Ωcm. As a passivation layer our «improved SiN_x» method has been used on both sides of the test wafers with boron diffusion.

The best results obtained from each group of this investigation are shown in table III. A very poor performance is obtained for inline belt furnace diffusion of boron emitters, with only a slight advantage for diffusion from liquid boron source. An effective lifetime of only 22-25 µs and an implied V_{oc} of not higher than 581 mV indicates that substantial contamination occurs during diffusion in the belt furnace [8,9]. This is further strengthened by the results of tube furnace diffusion of boron paste or liquid, which shows up to a factor 4 higher lifetime and an implied V_{oc} higher by more than 35 mV. In this case the tube furnace was used only for the temperature step (drive-in).

Table III: Minority carrier lifetime (τ_{eff}), implied V_{oc}, and emitter recombination current density (J_{oe}) measurements of symmetric $p^+/n/p^+$ devices, measured using QSSPC at an injection level of 1×10^{15} cm^{-3} and after firing. The emitter sheet resistance varies between different diffusion processes from 50-65 Ω/square.

Diffusion process	Boron source	τ_{eff} [µs]	Implied V_{oc} [mV]	J_{oe} [fA/cm^2]
belt	paste	22	565	870
tube	paste	74	607	700
belt	liquid	25	581	2100
tube	liquid	101	615	800
tube	BBr_3	600	670	65

However, a far better performance is obtained for BBr_3 diffusion. This can probably be understood by the fact that the quartz tube furnace diffusion using BBr_3

liquid bubbled by N_2 does not have any metal inside the tube, in contrast to the belt furnace, and, additionally, it does not use either paste or liquid sources of boron which are more likely to incorporate unexpected contamination. As a result, the BBr_3 diffusion results in a much more contamination-free p^+-emitter. This is clearly rewarded at the device level, as can be seen by a factor of ten lower emitter recombination current density. Such a low recombination current density of the boron emitter agrees well with literature values [4,11]. Work is underway to quantify these differences also at the cell level.

2.3 Solar cell development on n-type mc-Si wafers.

Having identified the importance of a clean B-diffusion, we can continue the development of the n-type multicrystalline process. Among the various ways of diffusing boron into n-type silicon, as described in the previous section, the emphasis was put on BBr_3 diffusion since it was proven to be by far the most promising method. Compared with the lifetime test samples (symmetric $p^+/n/p^+$) fabricated for the purpose of investigating junction and passivation quality, the solar cells based on n-type substrates must have a n^+ (phosphorous) diffusion for a BSF, along with the boron diffusion for the emitter, in order to facilitate the formation of an Ohmic contact for the base metallization. We found that the best results are obtained when the phosphorus BSF layer is diffused simultaneously with the BBr_3. Other great advantages of simultaneous diffusion are that it shortens the total process time. A schematic layout of such solar cell is shown in figure 2. In-situ oxidation was performed after the BBr_3 diffusion, in order to remove the Boron Rich Layer (BRL) which is formed during BBr_3 diffusion [12]. Figure 3 shows the resulting boron (emitter) doping profile measured on a polished FZ test wafer, using the Electrochemical Capacitance-Voltage (ECV) method. The ECV measurements reveal a doping profile of boron up to 0.2 μm depth with a visible surface depletion region. This depletion could be caused by the in-situ oxidation performed to remove the BRL. Further optimization seems to be needed in order to avoid this depletion region, which could enhance surface recombination of the minority charge carriers in the p^+ emitter because of an unfavourable electric field direction.

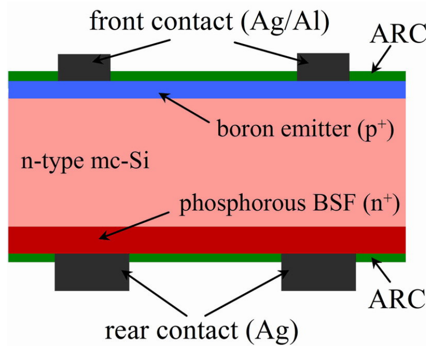

Figure 2: Schematic cross-section of our n-type solar cells.

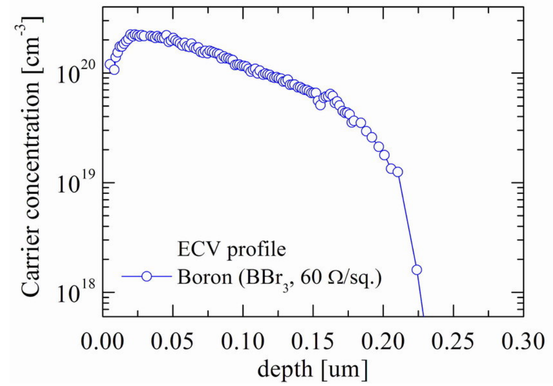

Figure 3: Diffusion profile for boron (emitter) measured by ECV method on polished FZ-Si wafer.

2.4 Optimal base resistivity

In the following we have investigated solar cells fabricated on wafers belonging to different n-type mc-Si ingots with difference in their base resistivity, with the purpose to find out the optimum resistivity range for n-type mc-Si ingots and cells. Two mc-Si n-type ingots have been selected for this investigation: a compensated ingot (called ingot 5) which is partially p-type (boron) and partially n-type (antimony) doped. Such a compensated ingot is very well suited for this type of investigation as it allows for a large variation in wafer resistivity on a narrow part of the ingot size while variation in concentration of metal impurities and crystal defects is relatively small. The other n-type ingot (called

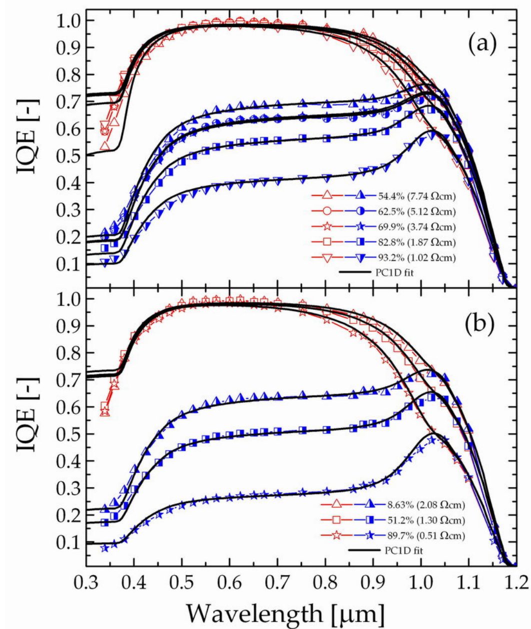

Figure 4: Internal quantum efficiency for front (empty symbols) and rear side (semi-filled symbols) illumination of solar cells selected from ingot 5 (a) and ingot 6 (b). The legend indicates the wafer's resistivity as well as its position towards the top of the respective ingot. The solid lines represent the PC1D calculation.

ingot 6 /antimony doped) that we have investigated has resistivity ranging from 2.2 to 0.3 Ωcm from bottom to top of the ingot. Solar cells have been fabricated (using the process described above) on 12.5×12.5 cm^2 wafers distributed to cover a resistivity range of 0.8 to 7.7 Ωcm from ingot 5 and 0.3 to 2.2 Ωcm from ingot 6.

Figure 4 shows the experimental IQE (symbols) of the solar cells fabricated from both ingots together with the PC1D fit (lines) using the measured front and rear doping profiles (emitter is shown in figure 3), surface reflection, base resistivity, and wafer thickness. The relevant fit parameters left for the modelling are the bulk lifetime, and the front and rear Surface Recombination Velocities (SRV). By fitting both front and rear IQE data all three fit parameters can be determined independently. The results show that only bulk lifetime is changed between various cells with a constant front SRV of $7.5(\pm0.5)\times10^4$ cm/s (on boron emitter) and rear SRV of $2.5(\pm1)\times10^5$ cm/s (on phosphorous BSF). A constant SRV is expected since all solar cells have been processed in the same run. This very good agreement between the model calculation and experiments, without any hidden fit parameters, enables us to quantify the required material characteristics to maximize the power conversion efficiency η of industrial n-type mc-Si cells. Figure 5 shows the bulk lifetime τ_b and minority carrier diffusion lengths L_d resulting from fitting the IQE data of the cells from both ingots investigated. It is observed that a resistivity higher than approximately 1.3 Ωcm is required in order to ensure L_d>W (W is the averaged wafer thickness of all investigated cells) for both ingots. For L_d<W, that means a resistivity<1.3 Ωcm, both ingots have almost identical lifetime even though this threshold occurs for wafers of >50% towards the top of the ingot 6 and only >85% towards the top of ingot 5.

Figure 6 shows the experimental conversion efficiencies and $J_{sc}\times V_{oc}$ product as a function of base resistivity for both ingots. As seen from the figure the best results are obtained for wafers belonging to ingot 6, with the highest performance obtained around 25% from the bottom of the ingot. The properties of the best cell measured are shown in table IV. To our knowledge, although not yet independently confirmed, this is the highest efficiency reported for an n-type mc-Si cell fabricated using an industrial process with screen-printed

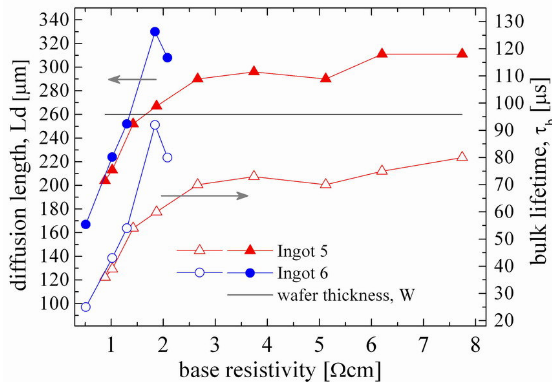

Figure 5: Minority carrier diffusion length L_d and bulk lifetime τ_b as a function of wafer base resistivity, determined from the PC1D fit of IQE data.

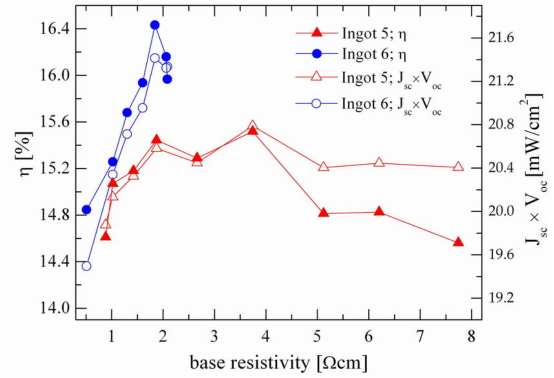

Figure 6: Experimental power conversion efficiency η and $J_{sc}\times V_{oc}$ product versus base resistivity of both mc-Si ingots investigated. Record high efficiency of 16.4% is obtained for wafers close to the bottom of ingots 6.

and fired-through metallization on large area (156.25 cm^2), outperforming even the current record of 16.1% for a laboratory process (4 cm^2; alkaline texture) [13]. This is a significant step forward for industrial production of solar cells based on n-type mc-Si feedstock. Moreover, further improvements are expected for this n-type mc-Si process, and work is underway to quantify and explore the potential benefits compared to the more developed and widely applied p-type process.

Table IV: Parameters of the best solar cell on mc-Si with an area of 156.25 cm^2.

Resistivity [Ωcm]	J_{sc} [mA/cm²]	V_{oc} [mV]	FF [%]	η [%]
1.84	35.2	607	76.7	16.4

Another interesting result that can be observed in figure 6 is that the $J_{sc}\times V_{oc}$ product continues to rise for cells made from ingot 6 as resistivity is increased while it stays rather constant for cells of ingot 5 for all wafers with L_d>W (resistivity>1.3 Ωcm). Above 3.5 Ωcm a decrease in efficiency of ingot 5 is, however, caused by a decrease in FF. This decrease in FF is a result of a higher series resistance caused by a non-optimised metallization grid of the base contact. Nevertheless, we show that the optimum base resistivity for n-type mc-Si feedstock lies between 1.5 to 4 Ωcm (these values can be lower if thinner wafers are produced) in order to maximize the efficiency output throughout the ingot.

3 CONCLUSIONS

A simple and cost effective method to passivate industrially produced p^+ (i.e., boron) doped emitters, based on PECVD SiN_x technology, has been developed. Compared with the more conventional SiN_x layer, used successfully to passivate n^+ (phosphorous) doped emitters, this new method has demonstrated an efficiency enhancement of more than 2% absolute for industrial n-type cell process. Concerning boron diffusion, we have obtained far better performance for a process performed in a quartz tube furnace using tribromide (BBr_3) liquid bubbled source than using printed or spin-on sources, or a conveyor belt furnace.

We have demonstrated a process to fabricate n-type

solar cells on large area (156.25 cm^2) multicrystalline substrates, involving simultaneous diffusion of phosphorous BSF and BBr_3 emitter, screen-printed metallization and firing through, leading to a new record efficiency of 16.4%. Moreover, in experiments performed on wafers of different base resistivity show that the optimum target resistivity for n-type multicrystalline silicon wafers lies between 1.5 to 4 Ωcm (these values can be lower if thinner and/or higher quality wafers are produced) in order to maximize the efficiency output thorough the ingot.

ACKNOWLEDGEMENTS

The authors would like to thank ECN colleagues for assistance and advice, and to Lucilla Bittoni (Chimet Spa) for the generous supply of the front side metallization paste. ECN acknowledges co-operation with Tempress. This work was supported by the European Commission within the FoXy project under the contract number 019811(SES6).

REFERENCES

[1] D. MacDonald, L.J. Geerligs, Applied Physics Letters, 85, (2004) 4061.
[2] J.E. Cotter et al., 15th Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes (2005) 3.
[3] R. Petres et al., Proceedings of the 15th International Photovoltaic Science and Engineering Conference (2005) 128.
[4] J. Libal et al., Proceedings of the 20th European Photovoltaic Solar Energy Conference (2005) 793.
[5] J. Libal et al., Proceedings of the 31st Photovoltaic Specialists Conference (2005) 1209.
[6] R. Kopecek et al., Proceedings of 4th World Conference on Photovoltaic Energy Conversion (2006).
[7] M. Kerr, PhD thesis, Australian National University, Canberra (2002).
[8] F. Recart et al., Solar Energy Materials and Solar Cells 91, (2007) 897.
[9] D. Macdonald et al., Proceedings of 4th World Conference on Photovoltaic Energy Conversion (2006) 952.
[10] L.J.J. Tool et al., Proceedings of the 19th European Photovoltaic Solar Energy Conference (2005) 970.
[11] A. Cuevas et al., Proceedings of the 14th European Photovoltaic Solar Energy Conference (1997).
[12] M.S. Bae, PhD thesis, Columbia University, New York (1979).
[13] J. Libal et al., Proceedings of the 22nd European Photovoltaic Solar Energy Conference (2007).