A 500-dpi AC Capacitive Hybrid Flip-Chip CMOS ASIC/Sensor Module for Fingerprint, Navigation, and Pointer Detection With On-Chip Data Processing

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***Abstract*—A fingerprint detection technology that supports navigation, pointer, and fingerprint acquisition is described. The hybrid system consists of a silicon sensor substrate flip-chipped onto a mixed-signal ASIC. The sensor is linear and the finger is swiped over to scan the fingerprint. The navigation and pointer functions are based on the motion detection of the finger on the substrate sensor. Stroking and tapping the sensor substrate surface with the finger determines movement of the cursor and clicking-like mouse. To achieve 500 dpi fingerprint detection accuracy, separate process optimization for both the ASIC and the sensor substrate gives an alternative solution compared with all other silicon sensor approaches. The ASIC is 18 mm^2 in 0.25-μm CMOS and the sensor is 105 mm^2.**

***Index Terms*—CMOS ac capacitive fingerprint sensors, hybrid biometric system, navigation and pointer functions, intelligent sensors, mixed analog–digital integrated circuits.**

I. Introduction

BIOMETRICS can be defined as the analysis of physiological or behavioral characteristics to verify or identify a person for a particular reason. Each biometric technology has its strengths and limitations. No single biometrics is expected to effectively meet the needs of all the applications. There are around 14 different biometric techniques that are either widely used or under investigation. These techniques include: face, fingerprint, hand geometry, keystroke dynamics, hand vein, iris, retinal pattern, signature, voice print, facial thermograms, odor, DNA, gait, and ear recognition. Among all the biometric technologies, fingerprint sensing is the one that currently has received most researchers' attention, due to its technical capabilities and low-cost solutions.

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A number of CMOS sensor chips for fingerprint identification have been designed. They are matrix two-dimensional (2-D) sensors that require a large silicon area (30 to 225 mm^2), which makes it difficult to embed these chips in small devices [1], [2], [5]–[7], [9].

This paper describes a novel hybrid flip-chipped CMOS ASIC/sensor that uses biometric techniques to implement a three-in-one device that supports navigation, pointer, and fingerprint detection with on-chip data processing. The paper is organized as follows. First, a new hybrid sensor is proposed in Section II, together with the principle of operation. In Section III, the architecture of the hybrid system is described, along with details of the circuit implementation and the solutions used to address the systems constraints. The experimental results and the characteristics of the module fabricated using a low-cost passive silicon substrate flip-chipped to the CMOS ASIC are presented in Section IV. Section V draws the conclusions.

II. Hybrid Approach

A hybrid module consisting of a silicon sensor substrate, flip-chipped to a high-density small-size mixed-signal CMOS ASIC is presented in this paper.

The architecture integrates three functions: fingerprint, navigation, and pointer detection. During the fingerprint detection mode, the finger is swiped over the module, the fingerprint pattern is detected, and an image of the fingerprint is generated. In the navigation mode, the swipe sensor is used for four-directional navigation (up–down and right–left). The mode is dedicated for character-based displays. In the pointer mode, the swipe sensor is used as a pointing device or mouse. If a user moves a finger across the sensor surface, the velocity and the direction of the finger movement is calculated. This enables the user to move a cursor on a graphical display. In both navigation and pointer modes, it is possible to recognize a finger being tapped onto the sensor surface. Thus, single tapping and/or double tapping can be used for selecting objects and menus.

The module combines linear scanner ac-capacitive fingerprint sensor technology [3] with ASIC and flip-chip technology, and provides both scan-type fingerprint access control and pointer functionality for on-screen point-and-click navigation.

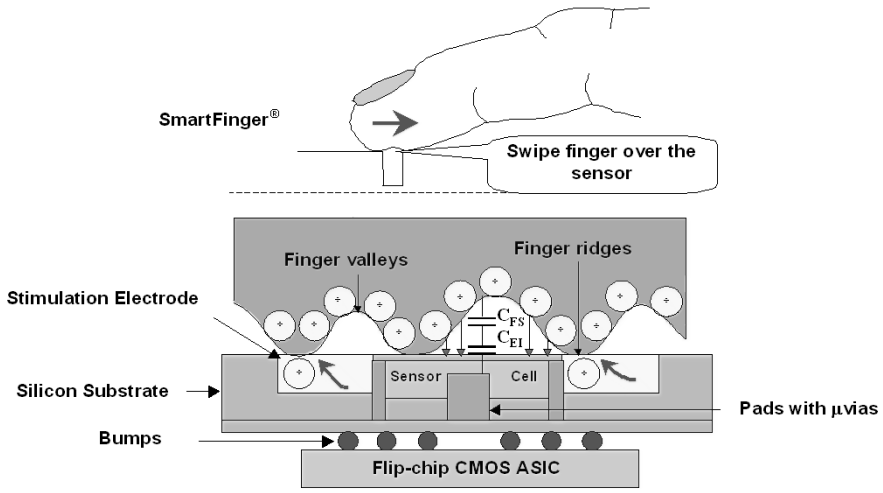


Fig. 1. Hybrid sensor principle of operation.

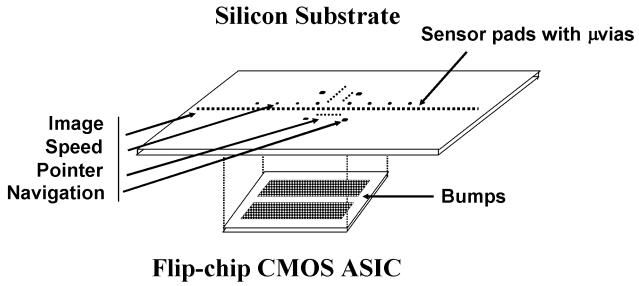
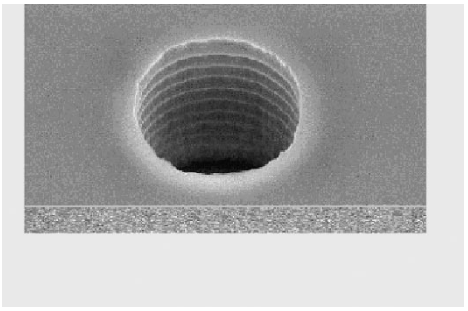


Fig. 2. Cross section of the module.



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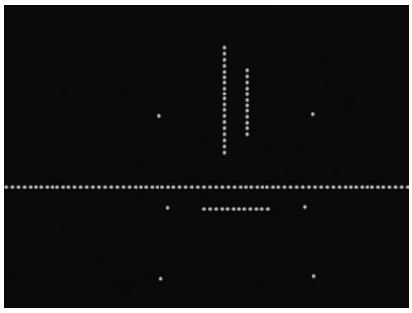


(b)

Fig. 3. Substrate with microvias for sensor connections.

The approach uses an optimized solution for these technologies, resulting in a cost-effective module.

The sensor consists of a linear structure of metal plates covered with a thin mechanically strong dielectric layer. Unlike previous designs, the sensor is implemented as a linear scanner, and the ASIC has to process only 256 channels. This approach reduces considerably the ASIC silicon area. The finger is stimulated by an ac signal via the stimulation electrode, and each sensor plate measures the modulated signal, which is proportional to the variable capacitance C_{FS} due to the pattern of ridges and valleys, as presented in Fig. 1. The capacitance is measured as the change in voltage that results when a fixed carrier frequency is modulated by the capacitance variations of the fingerprint pattern. As a user pulls a finger over the module, the sensors in the row measure the capacitance of each contact point of the finger surface with the sensor. Additional sensors are used to detect the speed of the finger movement, and when this single sensor line is sampled many times, a reconstructed image with equal scaling in both axes (50 μm) can be constructed. Fig. 2 shows a cross section of the module. The sensor is implemented by using a low-cost, passive silicon substrate. The connections of sensor elements placed on the top side to the back side of the substrate is realized by using miniature holes or microvias with 20-μm diameter and 50-μm pitch. The use of microvias simplify the routing and reduce the number of metal layers used by the sensor substrate. A microvia and the substrate illuminated from the backside in order to see the microvias are shown in Fig. 3.

The movement of the finger is detected by analyzing the motion of the pattern generated by ridges and valleys on sensor cells implemented for navigation and pointer functions.

III. Chip Architecture

At the architecture level, the partitioning of analog and digital processing is the key to reducing the silicon area and achieving low power consumption. The fingerprint/navigation/pointer ASIC architecture is shown in Fig. 4.

A. Analog Core

The analog module is implemented as a set of channels, each corresponding to one pixel of the sensor. The input signal is generated when the finger establishes a connection between the

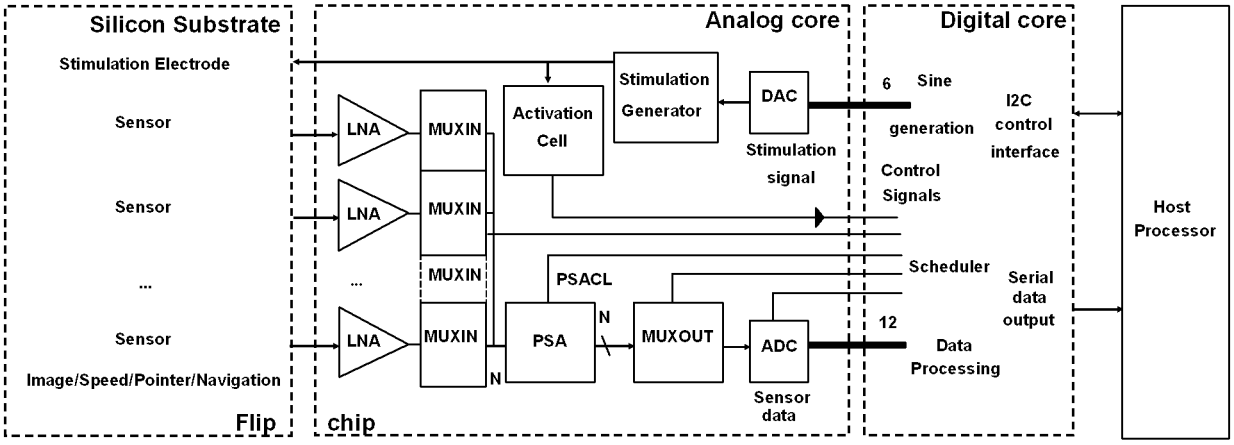


Fig. 4. Module architecture.

stimulation electrode and the sensor. The ac signal is a sine wave (65–160 kHz), generated internally.

1) Stimulation Generator: The stimulation signal is a digitally synthesized signal with 7-bit resolution (± 50) and 7.2° steps. Phase shifting is used to dynamically find the best sampling operating point. With a nominal 16-MHz system clock, the frequency is selectable as either 80 or 160 kHz. The digitized sine is given a dc offset before being passed through an 8-bit digital-to-analog converter (DAC). The synthesis of the output voltage from individual increments causes a spectrum of harmonics, the amplitude of which is given by the quantization in the time and amplitude axis and may be calculated by Fourier analysis:

$$A_{2m+1} = \frac{4}{\pi} \cdot \frac{1}{2m+1} \cdot \sum^{2n_1-2} (a_i - a_{i-1}) \cdot \cos\left[(2m+1) \cdot \frac{(2i-1)}{2^{2n_1}}\right], \quad m = 0, 1, 2, 3$$

where

$(2m+1)$	harmonic number;
(A_{2m+1})	amplitude of the $(2m+1)$th harmonic;
n_1	number of bits in the time axis;
a_1, a_{i-1}	amplitude of the ith and $(i-1)$th increment.

The amplitude of the increments must be calculated separately according to the approximation method. Even harmonics, which are not expected from theory, can be caused by glitches in the DAC and are calculated by Fourier analysis in a similar manner:

$$A_m = \frac{2}{m \cdot \pi} \cdot \left[(a + (-1)^m \cdot b) + 2 \cdot (c + (-1)^m \cdot d) \cdot \cos\frac{m \cdot \pi}{6}\right] \cdot \sin(2 \cdot m \cdot \pi \cdot \delta), \quad m = 1, 2, 3$$

where $a, b, c,$ and d are the amplitudes of the glitches, and 2δT is the pulsewidth which is assumed to be constant for all transitions from one bit to the succeeding bit. In the case of equal amplitudes $a = b$ and $c = d$, only even harmonics occur, and the equation is reduced to

$$A_m = \frac{2}{m \cdot \pi} \cdot \left[a + 2 \cdot c \cdot \cos\frac{m \cdot \pi}{3}\right] \cdot \sin(4 \cdot m \cdot \pi \cdot \delta), \quad m = 1, 2, 3.$$

The harmonics are filtered by using a second-order low-pass filter (LPF).

Each channel consists of a low-noise amplifier (LNA) and a multiplexer as presented in Fig. 4. The LNA has high input impedance to match the impedance of the finger and reads the low-level electrical signals. The LNA operates at 2.5 V with an open-loop gain of typical 80 dB. A bias circuitry for the LNAs and the processing unit provides the bias currents.

The ASIC design is based on a novel concept of pyramidal multiplexing channels into a common analog bus (N lines), which is fed to an analog-to-digital converter (ADC) via a second multiplexer [4]. The first group of multiplexers (MUXIN) switches input channels synchronous to the start of a cycle period of the sinus generator. The second multiplexer (MUXOUT) selects one envelope at a time and forward it to the ADC, which converts N envelopes to a digital representation within one cycle period. The detection of the envelope of the signal representing the finger impedance is achieved by using phase-sensitive amplifiers (PSAs).

The PSA rejects parasitic signals and extracts the amplitude of the in-phase signal on every channel. By using a sampler-type PSA, the carrier signal is suppressed without using a multiplier and the associated filter. Instead, the modulated signal is sampled when it reaches its peak value. The fundamental of the output will be delayed by one-half cycle of the carrier because of the sampling process of the desired low-frequency signal. Since the signal is held until the next sample, its harmonic content is well reduced or self filtered, due to the aperture effect. By using a sampler-type PSA, an LPF is not required. The PSA is controlled by a strobe signal (PSACL), generated by the digital part. The digital block controls the PSACL phase in order to compensate the phase shifts, so the signal representing the finger impedance is sampled on the maximum amplitude.

2) Noise Issues: By using this technique, the signal sampling is modeled as a product of the signal by a train of very narrow unit amplitude pulses. In this case, if we sample with the carrier frequency the amplitude-modulated signal from the finger, we are in fact demodulating it. The trains of pulses (sample signals) have a comb-like frequency spectrum with many spectral windows that are open to noise. The spectrum of the sampled signal thus consists on the replication of signal spectrum at intervals of l/T. The noise contributed by the sampler is reduced by considering T as the period of the carrier

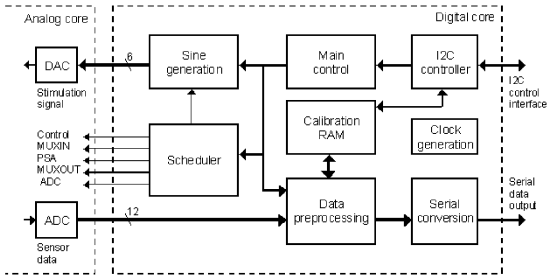
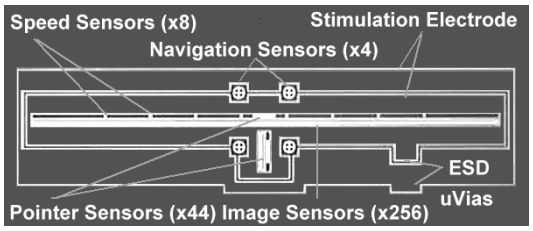
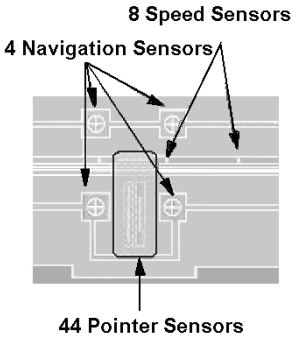


Fig. 5. Digital core architecture.



(a)



(b)

Fig. 6. Module topside micrograph.

frequency. By doing this, that synchronous sampling is, in fact, a synchronous demodulation with one frequency "window" that will give a dc component that is the output of interest. However, there is a window at frequency zero, and therefore, any low-frequency noise or interference superimposed on the signal will also result in a dc component that will add to the useful output signal. There is no series mode rejection. It is thus very important to place a bandpass filter before the sampler in order to prevent low-frequency noise and interference from entering the sampler.

In order to preserve the signal-to-noise ratio (SNR), we have implemented a bandpass filter formed by the input LNA and the sensor structure to ensure that the signal to be demodulated is filtered before the sampler.

The ASIC incorporates an activation cell that provides an activation signal used by the host device as an interrupt, indicating the point in time when a finger is detected on the sensor surface. When the skin approaches the sensor surface, it modifies the fringing field between the two metal plates facing the finger, reducing the effective impedance at the input of the detection amplifier. The cell ensures power control for operating the active circuit blocks. In the initial state, the sensor is in sleep mode, characterized by low power consumption with the activation cell waiting.

B. Digital Core

Fig. 5 shows a block diagram of the digital part. It is designed as a standard synchronous module, but to reduce power consumption, the clocks in some modules are stopped in some states. If the ASIC is operating as a fingerprint scanner, all sensors are processed. If it is used in pointer or navigation modes, only small subsets of the sensors are used and processed to reduce power and the amount of data delivered to the controlling microprocessor.

The digital module is composed of the following submodules.

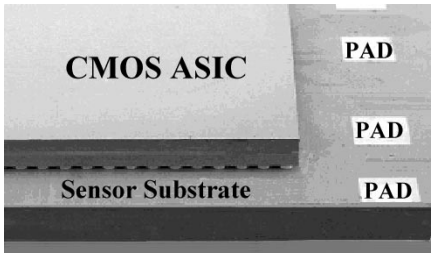
1) *I2C controller.* The chip is controlled by an external microprocessor through an I2C interface.
2) *Main control.* This module contains the main state machine that controls the various operating modes.
3) *Sine generation.* This module generates a digital sine for the stimulation signal. The sine samples are stored as a combinatorial table consisting of 50 samples of 7-bit width. By offsetting the start point of the sine generator, the phase of the sine can be adjusted in 7.2° increments. Two frequencies are available, nominal and doubled.
4) *Scheduler.* This is the timebase that generates all the control signals for the analog module, different for each operating mode.
5) *Calibration RAM.* This RAM stores calibration data for each individual sensor (dc offset and scaling factor). The calibration data can either be automatically generated by the chip in calibration mode, or it can be downloaded from the controlling microprocessor over the I2C control interface.
6) *Data preprocessing.* This module can operate in several processing modes.
   - In calibration mode, calibration factors for each sensor are calculated and stored in the calibration RAM. First, the dc offsets are obtained as sensor readings without input signal. Then scaling factors are calculated from sensor readings with an internally applied calibration signal. $\langle \text{Scaling factor} \rangle = \langle \text{programmable constant} \rangle / (\langle \text{sensor value} \rangle - \langle \text{dc offset} \rangle)$.
   - In normal operating mode, the following calculation is performed for each individual sensor: $\text{Normalized value} = (\langle \text{sensor value} \rangle - \langle \text{dc offset} \rangle) * \langle \text{scaling factor} \rangle$. Optionally, the full normalization can be switched off and raw sensor readings or dc normalized values $(\text{scaling factor} = 1)$ can be delivered.
7) *Serial conversion.* The data is delivered serially over a dedicated interface.

IV. Experimental Results

A. Characteristics of the Sensing Circuit

The system accepts various finger conditions including deviations of finger movements over the sensor. Software algorithms

(a)



(b)

Fig. 7. Module backside micrograph.

take into account these elements in order to achieve high identification accuracy and image enhancement. The sensor substrate and the image/navigation/pointer sensors on the topside of the module are shown in Fig. 6. The backside micrograph of the module with the flip-chipped ASIC/sensor is shown in Fig. 7. Performance is summarized in Table I.

A comparison of different swipe fingerprint sensors available today is presented in Table II.

B. Software Algorithms

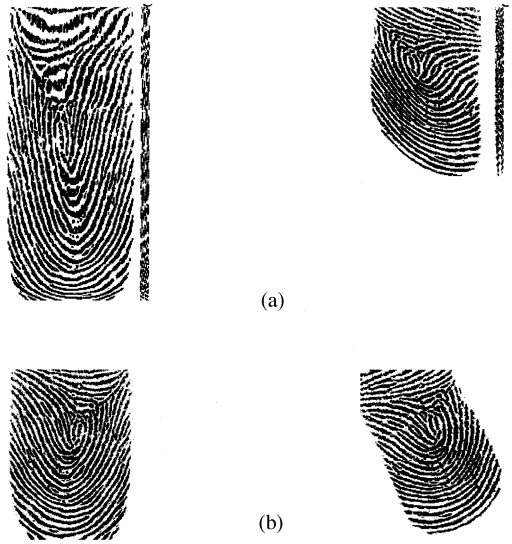
The software algorithms for fingerprint recognition, pointer, and navigation are compatible with the processing power of digital baseband processors used in mobile terminal design. Currently, all algorithms are ported to an ARM920 processor. However, in future generations, hardware implementation of real-time processes like the image reconstruction, pointer, and navigation algorithms will reduce the processor impact to a minimum. These three algorithms are the core algorithms of the hybrid module and will be described in more detail below.

1) Image Reconstruction: During the acquisition process, the swiping velocity and direction typically will vary from one swipe to the other. This introduces unwanted degrees of freedom into the images like skew, stretching, and compression. These degrees of freedom must be removed prior to authentication and identification.

The purpose of the reconstruction algorithm is simply to remove any distortions in the fingerprint images coming from a varying finger-swiping speed and direction. A correctly reconstructed image will be suitable for any fingerprint recognition algorithm taking into account translational and rotational degrees of freedom (see Table III). A repeatable geometrical reconstruction of the images would imply that all distances within images captured from the same finger do not vary by much. If this is the case, the images can be aligned by translation and rotation only. Almost any fingerprint-matching algorithm relies on this fact, and it is crucial for the biometric performance. To put it simply, the reconstruction algorithm calculates the distance traveled by

TABLE I
PERFORMANCE SUMMARY

Sensor size (external area):	105 mm^2
Sensing area:	3.25 mm^2
CMOS ASIC size:	18 mm^2
Image resolution:	500dpi
Operating voltage:	analog 2.5V, digital 1.5V
ESD resistance:	>15kV
Operating temperature range:	-20 to 70 °C



(a)

(b)

Fig. 8. Results of reconstructing two images of the same finger. (a) Before reconstruction algorithm. (b) After reconstruction algorithm.

the finger in real time and adds rows to the reconstructed image at every time instant the finger has moved 50 μm, ensuring at least 500-dpi resolution in both the pulling direction and along the sensor line.

Fig. 8 illustrates the purpose of the reconstruction algorithm. Two fingerprint images of the same finger captured by the hybrid device are shown. The figure shows automatic gain and offset normalized images. The two upper images are unscaled, whereas the two lower images are reconstructed. After image reconstruction, the two images can be aligned and compared directly by allowing for translational and rotational degrees of freedom. Image skew, stretching, and compression are removed by the reconstruction algorithm.

2) Pointer and Navigation: The fingerprint swipe sensor can be used as a pointing device (as a mouse). If a user moves a finger across the sensor surface, the velocity and the direction of the finger movement is calculated. This enables the user to move a cursor on a graphical display. For character-based displays, the pointer can be used for four-directional navigation (up–down and right–left). The pointer is also able to recognize

TABLE II
SWIPE SENSOR IMPLEMENTATIONS AVAILABLE TODAY

	NTT	Fujitsu MBF300	Authentec AES2500	Atmel FingerChip™	ST SmartFinger®
Fingerprint image	Yes	Yes	Yes	Yes	Yes
Navigation function	No	No	Yes	No	Yes
Pointer function	No	No	No	Yes	Yes
Image resolution (dpi)	508/500	500	500	500	500
Technology	0.25μm CMOS 3M	0.5μm CMOS	0.35μm CMOS	0.8μm CMOS	0.25μm CMOS 5M
Sensing area (mm^2)	143.36(11.2x12.8)	21.76 (1.7x12.8)	7.89 (0.81x9.75)	5.6 (0.4x14)	3.25 (0.25x13)
Substrate area (mm^2)	-	60.2 (4.3x14)	69 (5x13.8)	239.4 (9x26.6)	105 (7x15)
Silicon area (mm^2)	225 (15x15)	29.9 (2.3x13)	30 (3x10)	29,41 (1.7x17.3)	18 (4x4.5)
Measurement method	DC capacitive Array (224x256)	DC capacitive Array Swipe (32x256)	AC capacitive Array Swipe (16x192)	Thermal Array Swipe (8x280)	AC capacitive Linear Swipe (1x256)
Power Supply	2.5V	3.3/5V	2.4/3.6V	3/5.5V	2.5V Analog 1.5V Digital

TABLE III
PROPERTIES OF THE IMAGE RECONSTRUCTION ALGORITHM

Swiping speed range	0-56.6 cm/s
Swiping angle tolerance	±20 °
Processing power	Application dependent

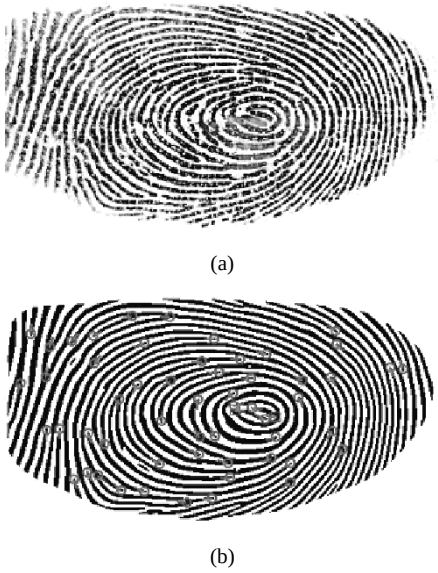
TABLE IV
PROPERTIES OF THE POINTER ALGORITHM

Swiping speed range	0-56.6 cm/s
Resolution	0.2 mm (configurable)
Processing power	Application dependent

a finger being tapped onto the sensor surface. Thus, single tapping and/or double tapping can be used for selecting objects and menus.

The pointer works as a miniaturized touch pad. However, displacement is defined by measuring finger swiping speed and direction instead of position. This is possible by spatio-temporal pattern matching of the signals from the finger. The underlying algorithm is quite similar in nature to the image reconstruction algorithm, but it checks for motion in all directions (see Table IV).

The pointer makes the hybrid approach unique and utilizes a single module for fingerprint recognition and on-screen pointing and navigation. The module eliminates the use of additional buttons and would be of great advantage for small handheld devices like mobile phones and PDAs.



(a)

(b)

Fig. 9. Fingerprint image from image-sensing circuits. (a) Automatic gain and offset normalized image. (b) Binary image with extracted features overlaid.

A fingerprint image captured by the hybrid device is shown in Fig. 9. Fig. 9(a) shows an automatic gain and offset normalized image, while Fig. 9(b) shows a binary image with extracted features overlaid. The extracted features are the minutiae points, which can be stored and used during subsequent matching.

C. Testing and Biometric Benchmarking

The reconstructed images from the hybrid module have been run through a biometric benchmarking test. The measurements were performed on the hybrid module implemented using the first silicon sensor flip-chipped on the ASIC cut 1.0. An Automatic Fingerprint Identification System (AFIS) has been developed for this purpose. The AFIS is minutiae-based and consists

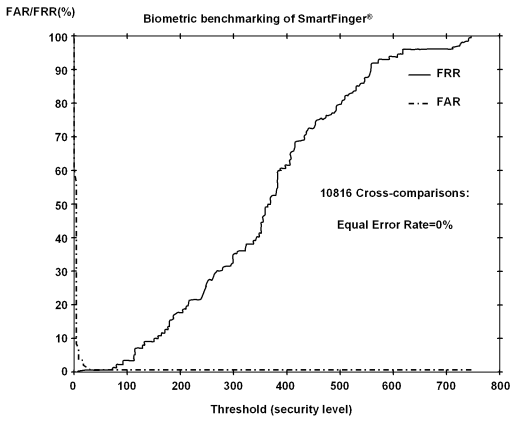


Fig. 10. Biometric benchmarking test of the hybrid module.

of two modules, one for minutiae extraction and one for minutiae matching. The algorithm allows for translational and rotational degrees of freedom. Fig. 10 shows the results from the biometric benchmarking test of the hybrid module. During the benchmarking test, four images of two different fingers from 13 individuals were captured with the hybrid sensor. The images were reconstructed in real time. All 104 images were cross matched (10 816 cross comparisons). The dashed curve shows the false acceptance rate (FAR), and the continuous solid curve shows the false rejection rate (FFR). The equal error rate (EER) $= 0\%$ is defined as the level at which the two curves cross and ZeroFar $= 0\%$ is defined as the lowest FRR at FAR $= 0\%$. For threshold values less than 30, false acceptances occur. For threshold values between 30 and 70, no false acceptances and no false rejections occur. For threshold values above 70, false rejections are observed. In the demo application for the hybrid module, the threshold value is set to 60.

The tests give only a rough estimate of the true FAR and FRR. The true EER for a larger population is expected to be somewhere between 0 and 0.01%.

V. Conclusion

An evolving biometric system based on a novel hybrid module architecture that enables fingerprint navigation and pointer functions to be integrated on a CMOS mixed-signal analog–digital ASIC flip-chip to a silicon substrate has been presented.

The key feature is a new design methodology and architecture and circuit concept for the pyramidal multiplexing of the channels into a common analog bus. When the user swipes the finger on the chip, the fingerprint patterns are detected with an array of capacitive sensors, and a mixed analog–digital circuit detects the motion of the pattern. The information is used for reconstructing the fingerprint pattern or for detecting the direction of movement of the finger across the surface of the sensor.

This enables reducing the silicon area and the analog circuitry considerably. Separate sensor and ASIC optimization paths are used in order to reduce the overall cost of the module.

The sensor substrate plate is covered with a hard film to prevent physical and chemical damage, and thus, robust mechanically strong operation is provided.

The ASIC was implemented using a 0.25-μm double-poly five-metal CMOS. The small size (18 mm^2), compared with other implementations (147 mm^2) [1], allows future additions of embedded processor on the chip, while keeping the low cost of the module. The proposed architecture enables a hybrid solution (linear ac-capacitive fingerprint silicon sensor substrate, CMOS ASIC and flip-chip) to be implemented on a single module. This architecture provides, for the first time, a system that integrates three functions: fingerprint, navigation, and pointer detection. The experimental results demonstrate the effectiveness of the architecture. When the user swipes his/her finger on the chip, the fingerprint patterns are detected with an array of capacitive sensors, and a mixed analog–digital circuit detects the motion of the pattern.

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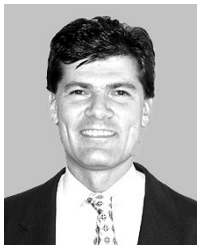

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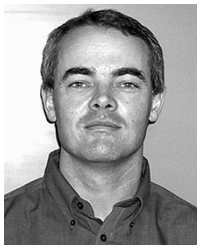

Laurent Le Pailleur was born on June 9, 1965, in Bayeux, France. In 1989, he received the M.S. degree in electrical engineering from the Ecole Nationale d'Ingénieur, Caen, France. He also received the M.S. (DEA) degree in instrumentation and automation and the M.B.A. (DESS) degree from Caen University.

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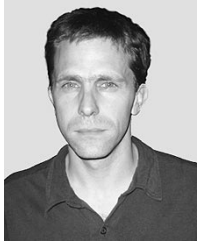

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