The European 3D Technology Platform (e-CUBES)

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INTRODUCTION

The European 3D technology platform that has been established represents the ensemble of 3D integration technologies which were developed within the e-CUBES project (6th European Framework ICT). The work was focussed on the requirements coming from application demonstrators. However, other requirements set by taking the visionary approach of developing ultra-miniaturized micro/nano-systems were also a major task of the work. Seven corresponding technologies were successfully developed building a European platform on 3D Integration. These are in the 3D integration categories

Vertical System Integration (3D-SOC): Fraunhofer IZM-M’s Through-Si Via (TSV) Technology (ICV-SLID) and SINTEF’s Hollow Via & Gold Stud Bump Bonding (HoViGo),

Chip Stacking (3D-WLP): IMEC / Fraunhofer IZM’s Thin-Chip-Integration Technology (TCI/UTCS) and

CEA-LETI’s Via Belt Technology, and

3D Assembly (3D-SIP): 3D-PLUS’ High Performance Package-in-Package (HiPPiP) and Wireless Die-on-Die (WDoD) Technologies, and Tyndall’s Submicron Wire Anisotropic Conductive Film Technology (SW-ACF).

Four optimized 3D integration technologies were successfully used in the development of three e-CUBES application demonstrators: Thin-Chip-Integration technology (TCI/UTCS) for Philips’ Health & Fitness demonstrator, TSV technology ICV-SLID and HoViGo for Infineon’s Automotive demonstrator (TPMS) and Package-in-Package technology HiPPiP for Thales’ Aeronautic demonstrator.

3D INTEGRATION TECHNOLOGIES

A technology platform has been established within the European Integrated Project “e-CUBES”. It became evident that the fabrication of heterogeneous systems with the need for miniaturization can only be realized by system integration technologies which use the third dimension. The main objective was to provide 3D integration technologies which on the one hand increase the performance sufficiently and at the same time allow for cost-efficient fabrication in order to achieve products with a large market potential. 3D-SOC based on bonding and vertical inter-chip wiring of stacked thinned device substrates using freely positioned (area) through silicon vias (TSVs), 3D-WLP of embedded devices by wafer-level packaging (without TSVs) and 3D-SIP of packaged devices (without TSVs). Suitable technologies in all these three main areas of interest for heterogeneous system integration were developed building the established European technology platform (published online in terms of technology summary sheets: http://ecubes.org). The 3D technologies are selected and optimized concerning the availability of devices (packaged dies, bare dies or wafers) and the requirements of performance and form factor (see Fig. 1). The processes and key characteristics of these technologies are described in the following sections.

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Fig. 1: The European 3D Technology Platform
Through Silicon Via Technology ICV-SLID

Targeting on heterogeneous systems with high-performance and small form factor requirements, a post backend-of-line 3D-SOC technology based on TSVs and stacking of devices by intermetallic compound bonding has been developed and evaluated. The chip-to-wafer stacking process is optimized for 3D integration of known good dies. The through silicon vias are fabricated on completely processed bare device wafers. High aspect ratio TSVs through all BEOL layers and typically 10 - 50µm deep into the Si substrate are isolated with a highly conformal O₂/TEOS oxide and void-less filled with tungsten or copper CVD. The thinned top chips are connected to the bottom device wafer by the SLID metal system (Cu, Cu₃Sn, Cu). The Cu/Sn metallization for the SLID interconnect is realized using through-mask electroplating. The copper and tin thicknesses are selected according to the temperature profile during bonding with respect to the topography of the devices. During bonding at 270 - 300°C the deposited Sn is completely transferred into Cu₃Sn intermetallic compound. This ε-phase is thermodynamically stable with a melting point above 600 °C. Using appropriate film thicknesses, tin is consumed and the solidification is completed within a few minutes, leaving unconsumed copper on both sides. The TSVs are interconnected by Al wiring to the metallization of the top device and by the above described SLID metal system to the metallization of the bottom device. The vertical interconnect resistances are approx. 0.2 Ohm for 3 x 10 x 50 µm dimensions including SLID contact. The minimal pitch achieved for TSVs is typically 10µm. For chip stacking with high-resolution alignment a minimum SLID pad size of 5 x 5 µm² is required. Depending on the alignment accuracy, the pitch of the complete vertical interconnects (TSV and SLID) is 10⁴ - 10⁵ cm⁻². A pitch reduction down to 3 µm is feasible and enables interconnect densities of 10⁶ cm⁻².

A schematic of the 3D stacking concept exemplifying the modular chip-to-wafer principle of the ICV-SLID technology is shown in Fig. 2, left. Cross section of a 3D integrated test chip with W-filled TSVs and Cu/Sn SLID bond (mid) and IV-characteristics of a TSV-interconnected MOS transistor in the top device layer (right) demonstrate the successful integration of functional 3D-ICs.

Fig. 2: Post-BEOL TSV Technology ICV-SLID

For the application of heterogeneous system integration, in the majority of cases the components are available as fully fabricated devices only. In consequence ready-processed and thinned devices with different backend-of-line compositions (metals/dielectrics compound on thin silicon) have to be stacked. The enabling processes show up as especially sophisticated when studying the production requests (e.g. TSV formation on completely processes device wafers with complex BEOL layer structures). The basic conditions for the application of intermetallic compound bonding have to be considered carefully. Two of the critical topics are the topography of the devices to be stacked and the possibility of getting high mechanical stress built into the final 3D-IC stacks due to the TSV formation and/or the bonding process. Corresponding process optimization was required to overcome these limiting conditions. The optimized ICV-SLID technology was successfully applied for the fabrication of Infineon’s TPMS wireless sensor node [1]. The key element of the TPMS, a 3D-IC / MEMS stack, consists of a microcontroller, an RF receiver and a pressure sensor from Sensoron and was processed in combination with SINTEF’s MEMS-specific 3D integration technology which is described below.
Hollow Via & Gold Stud Bump Bonding (HoViGo)

Micro- and nano electromechanical (MEMS/NEMS) devices often rely on the substrate thickness for stability, reliability and strength. Whereas most 3D integration technologies for logic and memory ICs are based on substrate thinning, a different approach is clearly required for MEMS/NEMS. The high topography of the surfaces is a general challenge for the processing and the use of wet processing methods in particular is often problematic in the presence of inlets and released structures. When certain functional and nano materials are involved, low temperature processes are required. These are amongst the technological challenges addressed by SINTEF’s Hollow Via and Gold Stud Bump Bonding (HoViGo) technologies [2], developed within the e-CUBES project.

The Hollow Via technology allows the fabrication of TSVs in 300 to 1000 µm thick silicon substrates. Using Bosch deep reactive etching (DRIE), 20 x 50 µm or 50 x 50 µm holes are etched through the silicon wafer. A high quality thermal oxide is grown onto the sidewalls of the DRIE holes thereby providing electrical isolation of the TSVs. Low pressure chemical vapour deposition of a thin conformal polysilicon layer is done to provide a conductive layer through the vias, followed by phosphorous gas phase doping to reduce its resistance. Metallization is then sputtered on both sides of the wafers. As the holes are not being filled, conventional spin coating of resist cannot be used to pattern the conductive layers. Instead, a 15 µm thick photosensitive resist film (MX-5015 from Dupont) is laminated onto the wafers and the film is patterned by photolithography in order to serve as an etch mask for etching the metal and the polysilicon. For the 20 x 50 µm via holes the minimum via pitch is 110 µm while it is 140 µm for the 50 x 50 µm holes. Depending on the wafer thickness and via hole size, the pitch can be further reduced to 50 µm. The resistivity per TSV depends on the via size, wafers thickness and polysilicon thickness, but it is typically below 10 Ω. Reliability tests including temperature cycling from -40 °C to +150 °C and storage for 30 min at 260 °C show excellent results. Promising applications for the hollow via technology include the fabrication of TSVs in MEMS device and cap wafers, radiation detectors and silicon interposers.

For the automotive demonstrator within e-CUBES, SINTEF demonstrated that chip-to-wafer gold stud bump bonding is a technology ideally suited for 3D stacking of MEMS and application specific ICs (ASICs), in particular when there is a small number of I/O’s involved. Gold stud bumps are placed directly onto the metallised bonding pads of the MEMS device, without the need for any underbump metallization or electroplating. After bumping, the MEMS wafer is diced and the individual dice are flip chip bonded onto the ASIC wafer. Since there are no wet process steps involved, the presence of released structures or inlets is not a problem. The bonding can be done using thermocompression at 200 °C or by ultrasonic bonding at 120 to 140 °C, which makes it compatible with most functional materials and with CMOS devices. The minimum pitch demonstrated within e-CUBES was 90 µm, but it is believed that this can be scaled down to about 50 µm. Excellent shear strengths were measured, both with (> 50 MPa) and without (> 25 MPa) the use of an underfiller. Temperature cycling and high temperature storage test had no notable impact on the bonding quality. The fact that MEMS and ASIC often differ when it comes to wafer size, die size and yield, makes the chip-to-wafer approach ideally suited for such heterogeneous 3D integration of devices.

TCI – Thin Chip Integration Technology

The embedding of 20 - 40µm thin dies into a BCB - copper multilayer thin film build-up on wafer level is the key technology of this 3D-WLP approach. A reliable thinning process on wafer level as well as adapted handling steps of the thinned dies are the basic requirements for the TCI technology (also called UTCS – Ultra Thin Chip Stacking). The photostructurable BCB polymer material acts as a glue layer as well as interdielectric layer and combines the advantages of a low k dielectric material and good planarization behavior. Electroplated Cu tracks...
are used for the electrical routing between embedded dies, wafer substrate and top metallization. For a successful implementation of the TCI technology the embedded chips have to be smaller than the base chip (heterogeneous integration). The TCI technology enables the shortest interconnections between embedded die and substrate chip. In addition to the realization of impedance defined interconnection lines this technology is well adapted for high frequency applications since it allows chip to substrate interconnections exhibiting extremely low parasitic capacitance and inductance together with very small bond pad pitches of future CMOS technologies. The final pad metal layer (Cu-Ni-Au) on top of the stack allows the connection to a PCB as well as mounting flip chip components or SMD components on top of the 3D stack. The process flow of the TCI technology is shown in Fig. 4.

![Fig. 4: Process flow of TCI technology](image1)

Within the European project e-CUBES the thin chip integration technology was used for the realization of the 3D stack of a prototype wireless activity monitor. Together with the project partners Philips Applied Research, IMEC and the University of Uppsala a silicon substrate with integrated µ-Processor and a 17 GHz transmitter chip was designed [3]. The wireless sensor node consists of a 3D silicon substrate which contains the thinned active chips in a BCB-Cu multilayer stack, an antenna coupling structure that interfaces to a patch antenna on the back of the substrate and SMDs including a 3D accelerometer on top. This silicon substrate is soldered to a PCB which also carries the power management electronics, a battery and a coil for wireless charging on the backside. The linear-polarized patch antenna, glued on the backside of the 3D silicon stack is fed by a 50Ω microstrip line using aperture-coupling through an H-shaped slot in the ground plane of the 3D silicon stack. After housing of the electronics, the wireless activity monitor sensor node has a size of only 20 x 11.4 x 7.4 mm³.

The active components, an MSP 430 µ-processor from TI and a 17GHz transmitter chip designed by Philips, were thinned to a thickness of 20 µm at the Fraunhofer IZM-M in Munich. These dies were glued onto a silicon substrate which already contains an electroplated ground metal layer, thin film resistors (NiCr and TaN) and Cu interconnects to the substrate. Using the above mentioned BCB-copper multilayer technology a 3D integrated system with a size of 8x18 mm² was manufactured on wafer level. The main features of this integrated 3D stack for the wireless sensor node are:

- Embedded MSP430 µ-processor and 17GHz transmitter chip (both 20µm thickness)
- 7GHz oscillator flip chip
- SMD crystal on top of embedded µ-processor
- Integrated passives: NiCr or TaN thin film resistors; Cu-BCB-Cu capacitors; a 7 GHz Balun
- Aperture-coupled antenna through an H-shaped slot
- 0201 SMDs and 3D accelerometer SMDs assembled on integrated Si substrate

The integrated 3D Si substrate after SMD assembly is shown in Fig. 6. The soldering of the integrated silicon substrate to the PCB as well as the housing of the whole sensor node was done at Philips Applied Technologies.
in Eindhoven. The functionality of the thinned active dies as well as the whole sensor node was successfully demonstrated.

![Image](image1.png)

**Fig. 6: e-CUBES 3D integrated TCI substrate for wireless sensor node fabricated at Fraunhofer IZM and final Health and Fitness Demonstrator assembled at Philips Applied Technologies**

**Via Belt Technology**

Leti’s Via Belt technique consists in making conducting pads around bottom die. This "belt" of pillars enables connection between the wafer rerouting and the back side of the die. Filling the spaces between the dies with a polymer achieves a smooth surface, leaving the top of the pillars favourable for contact connection of top dies.

In order to reduce manufacturing cost which is highly dependent on the number of steps, a specific process is implemented. The same seed layer is thus used for the connection circuit and for electrolytic growth of the pillars and μ-inserts. For this, the following 3D-WLP process flow is implemented:

- Continuous Ti/Cu base layer deposition, the Ti forming the bonding layer between the oxide and Cu.
- Growth of Nickel μ-inserts on the pre-determined host pads.
- Rerouting in the base layer. The patterns of this level have been specifically designed for all the host pads of the pillars to be connected to one another.
- The copper pillars are electroplated by means of a photo-patternable dry thick film.
- Dies N°1 are flip-chipped with a DATACON 2200 APM+ machine. After all the dies have been placed, a collective thermocompression stage is implemented to promote adhesion and connection between the dies and wafer (Fig. 7).
- After die attachment a specific polymer is spun to embed the chips and pillars, cured and then ground (Fig. 8).
- Then the photoresist layer is fully patterned with a mask including a 10µm hole at 15µm pitch. The isopotential patterned seed layer enables a third electro-deposition step to obtain a Ni μ-insert area localized at the top of the copper pillars.
- Finally dies N°2 are placed face-down to be connected to the copper pillars.

![Image](image2.png)

**Die 1 (4x4mm²) face-down**

![Image](image3.png)

**Fig. 7: Top view of a part of 200mm substrate after Copper pillar ECD and die 1 stacking**

![Image](image4.png)

**Fig. 8: Top view after epoxy glue embedding and grinding**

The set of stacked dies were tested by measuring the resistance between 4 connections (daisy-chain) located at the interface between the wafer and die 1 and two connections located at the interface between the copper pillars and die 2. The electrical results are obtained on one hundred 3D modules. Although the results are dispersed, it can be observed that a large proportion of the dies are functional.
This cost-effective, polymer-based integration technology is aiming to perform three-dimensional assembly of standard dies on wafer scale which allows using non processed bare dies. To do so, a technique is implemented in which ECD Ni µbump are used for face to face interconnection and ECD copper pillars surround the host pad of the die and enable the devices to be connected on 2 levels. The first prototype produced has given encouraging results. Developments are on-going to validate the base bricks necessary to produce a 3D module in which the dies are stacked vertically.

**HiPPiP – High Performance Package-in-Package Technology**

The HiPPiP technology has been developed by 3D-PLUS. The main steps of the process are the placement of plastic packages on an adhesive foil, then the overmoulding with epoxy resin. After the curing of the resin a thinning of active and back-side is performed permitting to reduce the thickness from 1.2 mm to 0.4mm. Then, redistribution layers are processed in order to build a fan-out from the sections of the gold wires of the packages and finally different levels are stacked and vertical interconnexion is performed according standard 3D-PLUS patented process.

The advantages of this technology are the possibility of integration of almost any plastic components or passive ceramic components or bare dies of different dimensions and technologies and also integration of components which have been fully tested and burn-in. Test of each Known Good rebuilt Wafer (KGRW) is performed before stacking permitting to reach a good final yield. The manufacturing is adapted to low volume and low cost thanks to simple manufacturing steps.

![Fig. 9: Description of the main process steps of HiPPiP technology](image)

**Wireless Die-on-Die Technology (WDoD)**

WDoD patented 3D-PLUS technology is based on the same concept that HiPPiP technology except that it is dedicated to bare dies, typical thickness 100 µm.

Process is described in Fig. 10 and Fig. 11:

First step is the adhesive lamination of silicon or glass carrier. Second step is pick, flip and place of die on tape (only KGD are used) with accuracy better than +/-5 µm. Then compression moulding of epoxy resin is performed followed by optional grinding in order to reduce the total thickness of the stack. After the KGRW are de-taped.

RDL (redistribution layer) is then processed: sequential deposition of photodielectric, photolithography, seed-layer PVD, pattern plating of copper-gold tracks.

After the electrical test of each KGRW, they are stacked using non-conductive glue. Dicing of the rebuilt and stacked wafers can be now performed, followed by plating of dicing street edges with electroless nickel or copper and gold.

Finally, direct laser patterning with pitches of 100 µm is performed, followed by final electrical tests.
Thanks to the possibility of stacking bare dies of different dimensions and technologies, WDoD is particularly adapted to SIP concept. The KGRW concept allows also stacking KGRW of WDoD technology and KGRW of HiPpiP technology permitting then to stack almost any type of components in a module. Bus-metal concept permits also to integrate easily on the external sides of the module, patterned antennas for RF applications. Within the European project e-CUBES, and for the manufacturing of the aeronautical demonstrator, as the availability of bare dies were limited, only the HiPpiP technology was used for two levels: memory and MAX levels. The use of this technology permitted to lower the total thickness of the demonstrator of 3 mm. Next steps would be the industrialization of this demonstrator with the use of WDoD technology for available bare dies which will permit to decrease the total thickness of several mm.

Submicron Wire Anisotropic Conductive Film (SW-ACF) for 3D assembly

Flip chip interconnect is a space efficient 3D assembly method, which can be achieved by using either solder or conductive adhesives. Solder flip chip in general is more reliable, but has miniaturization restrictions and requires an additional underfill process step. For these reasons conductive adhesives were targeted, in particular submicron wire anisotropic conductive film (SW-ACF) which is different from traditional ACF in that it has smaller conductive features and potentially can achieve higher interconnect densities. The SW-ACF contains 220 nm diameter wires, while standard ACF’s use micron scale conductive particles. Wires with <220 nm diameters are prone to wire sweep at the bonding stage and defects or shorts could occur, while electrical resistances also increase with decreasing wire diameters.

Various versions of SW-ACF can be fabricated dependent on the application requirement. Wire aspect ratios up to 1:114 can be achieved. Typical length of the wires is about 25 µm and the density is about 40 wires/ 100 µm². The metal wires can consist of composite metals to match with different bond pad metallization. The choice of metal will affect the required bonding temperature profile, and needs to be considered on a case by case basis. The metal wires are electrochemically grown in a polymeric template containing an array of empty pores. It will be necessary to have a metal seed layer on one side of the polymer template from which the wires can be grown. Depending on the choice of seed layer material and thickness and wire material it can be difficult to remove the seed layer without damaging the filled wire pores. Fig. 12 shows the cross section of a flip-chipped SW-ACF sample applied to a bumped chip and planar substrate. The detailed magnified areas of the cross section show the condition of the wires.
Fig. 12: Cross section of the flip chip bonded submicron wire anisotropic conductive film and the magnified areas of cross-section

SW-ACF leans itself well to scaling up and be used at wafer level assembly. However, a more efficient metallization scenario can be obtained by growing of the metal wires in the SW-ACF directly onto the bond pads. The bond pads need to be electrically connected for this. The critical assembly step will be in the plating lab or wafer fab for this process.

The concept has been demonstrated for 25 µm bond pads and with a 50 µm pitch, but higher densities should be feasible when using smaller test structures. If shorting is observed between bondpads, a lower wire density could be investigated. Electrical SW-ACF joint resistances have been achieved as low as 1.25 Ω. Gold wires grown onto a gold seed layer gives the best electrical results, but aluminium or copper wires onto a gold seed layer give less problems in removing the seed layer. An aluminium seed layer is the easiest to remove, but wire growth onto it is not ideal. For high frequency RF a sub-micron-wire based joint has higher impedance than a solid bump and is harder to control. From an application point of view SW-ACF interconnect is particular suitable for smaller pad sizes & pitches, but also for small I/O counts and wafer scale assembly.

CONCLUSIONS

3D integration technologies in three main categories – 3D-SOC, 3D-WLP and 3D-SIP – have been developed and optimized concerning the availability of devices and the requirements of performance and form factor for the fabrication of ultra-miniaturized micro/nano-systems. The ensemble of the e-CUBES partners’ technologies represents a comprehensive 3D technology platform for future applications of heterogeneous system integration.

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