3D Integration Technologies
For Miniaturized Tire Pressure Monitor System (TPMS)

- supported by the European Commission
  under support-no. IST-026461 e-CUBES

Nicolas Lietaer¹*, Maaike M. V. Taklo¹, Armin Klumpp², Josef Weber² and Peter Ramm²

¹SINTEF, department for Microsystems and Nanotechnology, Oslo, Norway
²Fraunhofer Institute for Reliability and Microintegration, Munich, Germany
Outline

- Introduction
  - Heterogeneous integration
  - European 3D technology platform
- e-CUBES automotive demonstrator (TPMS)
- Technology choices
- Hollow through-silicon vias
- Interconnect for sensor and BAR
  - Au stud bump bonding
  - Cu/Sn Solid-Liquid Interdiffusion
- TPMS demonstrator results
3D Integration

**Definition:**
Fabrication of stacked and vertically interconnected device layers

**Motivations:**

**Form Factor**
- Reduced volume and weight
- Reduced footprint

**Performance**
- Improved integration density
- Reduced interconnect length
- Improved transmission speed
- Reduced power consumption

“The Ultimate Goal: Repartitioning”  
(P. Garrou / MCNC)
3D Integration

**Definition:**
Fabrication of stacked and vertically interconnected device layers

**Motivations:**

**Form Factor**
- Reduced volume and weight
- Reduced footprint

**Performance**
- Improved integration density
- Reduced interconnect length
- Improved transmission speed
- Reduced power consumption

“More than Moore” Applications
- Integration of heterogeneous technologies
Technologies serve different applications

Legend:
- More Moore (scaling)
- More than Moore (non-scaling)
- Mixed

Bubble size = driver impact

Ref.: ETP Nanoelectronics, A.J. van Roosmalen, December 13, 2007
e-CUBES®

Self-organising wireless sensor networks to monitor the environment

Human sensing & interaction with environment

Human brain

‘More Moore’
‘Beyond CMOS’

Digital content
Complex Design (SoC)
Lots of software

Non-digital content
Hetero Integration
Lots of processes

SoC can be a component of SIP
3D Integration Technologies for e-CUBES

IZM-M: ICV-SLID
SINTEF: HoViGo

IMEC/IZM: UTCS, TCI
CEA-Leti: Via-Belt

3D-PLUS: WDoD, HiPPiP
Tyndall: SW-ACF

3D-SOC
3D-WLP
3D-SIP
e-CUBES Application Demonstrators

IZM-M: ICV-SLID
SINTEF: HoViGo

IMEC/IZM: UTCS, TCI

3D-PLUS: WDoD, HiPPiP

Infineon´s Automotive
Philips´ Health & Fitness
Thales´ Aeronautic
3D Integration – Definitions

Concept Categories:

- **Stacking of packages** (or substrates) (eq. to 3D-SIP)
- **Stacking of embedded dies without TSVs** (eq. to 3D-WLP)
- **TSV Technology** (Vertical System Integration) with TSVs
  - “vias last”
  - “vias first”
    FEOL, BEOL, post BEOL
    TSVs prior / post stacking
3D Integration – Definitions (2)

TSV Technology

(Vertical System Integration)

with TSVs

- **3D-IC**
  3D Integrated Circuit: stacking of transistor layers
  (at local interconnect densities)

- **3D-SIC**
  3D Stacked Integrated Circuit
  (very high TSV densities)

- **3D-SOC**
  3D System-On-Chip: stacking of devices
  (global level)
  - Fabrication of Heterogeneous Systems
3D-SOC
stacked dies with TSVs

3D-WLP
stacked embedded dies without TSVs

3D-SIP
stacked packages
3D-PLUS: WDoD, HiPPiP, … (Stacking of Packages)
# 3D Technology Platform (e-CUBES)

<table>
<thead>
<tr>
<th>Technology</th>
<th>e-CUBES Partner</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>3D-SOC</strong></td>
<td></td>
</tr>
<tr>
<td>Through Si Via (TSV) Technology (ICV-SLID)</td>
<td>Fraunhofer IZM Munich</td>
</tr>
<tr>
<td>Hollow Via &amp; Gold Stud Bump Bonding (HoViGo)</td>
<td>SINTEF</td>
</tr>
<tr>
<td><strong>3D-WLP</strong></td>
<td></td>
</tr>
<tr>
<td>Thin Chip Integration (TCI / UTCS)</td>
<td>IMEC &amp; Fraunhofer IZM</td>
</tr>
<tr>
<td>Via Belt Technology (µInsert)</td>
<td>CEA-Leti</td>
</tr>
<tr>
<td><strong>3D-SIP</strong></td>
<td></td>
</tr>
<tr>
<td>HiPPiP</td>
<td>3D-PLUS</td>
</tr>
<tr>
<td>Wireless Die on Die Technology (WDoD)</td>
<td>3D-PLUS</td>
</tr>
<tr>
<td>Submicron Wire Anisotropic Conductive Film (SW-ACF)</td>
<td>Tyndall</td>
</tr>
</tbody>
</table>
Objective of e-CUBES project:
develop wireless sensor networks with miniaturized sensor nodes
3 demonstrators: Health and fitness, Aeronautics and space, Automotive
Tire Pressure Monitoring System (TPMS) chosen for the Automotive demonstrator
TPMS building blocks

- MEMS pressure sensor (glass-Si-glass stack): 1.8 x 2.1 mm² (150 mm wafers, 900 µm)
- MEMS bulk acoustic resonator (BAR): 0.8 x 1.3 mm² (150 mm wafers, 200 µm)
- Transceiver ASIC (TX): 3.8 x 3.3 mm² (200 mm wafers, 60 µm)
- μ-controller ASIC (μC): 4.3 x 3.8 mm² (200 mm wafers, 700 µm)
- Antenna
- Battery
- Package

Technologies required:
- μC - TX interconnect
- TX - sensor / BAR interconnect
- TX TSVs
- Sensor TSVs

3D integrated miniaturized TPMS
Technology choices

Au stud bumps with adhesive
(alternative: SLID)

SnAg µbumps and underfiller or SLID

TSV with W

Source: SINTEF/FhG IZM-Berlin

Source: Kulicke & Soffa

Silicon-glass compound wafer with TSVs
(alternative: hollow TSVs)

Source: SINTEF/SensoNor/PlanOptik
Technology choices

- **Au stud bumps** with adhesive (alternative: **SLID**)
- **SnAg µbumps and underfiller or SLID**
- **TSV with W**
- **Au stud bumps** only (alternative: **SLID**)
- **Silicon-glass compound wafer with TSVs** (alternative: **hollow TSVs**)

Source: SINTEF

Source: SINTEF/SensoNor/PlanOptik

Source: Kulicke & Soffa

Source: Fraunhofer IZM-Munich
SLID: Solid-Liquid Inter-Diffusion

Simultaneous formation of **electrical and mechanical** connections

- **Patterned electrodeposition**
- Contact under pressure and heat ~ 5 bar, 260 – 300 °C (Sn-melt)
- Formation of intermetallic compound; T_melt > 600 °C

Source: VSI project, funded by German Ministry for Education & Research (BMBF)
Chip-to Wafer Stacking by ICV-SLID Technology

- Fabrication of Tungsten-filled Inter-Chip Vias on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of Plugs
- Through Mask Electroplating
- Chip/Wafer Alignment and Soldering
## Through Si Via Technology (ICV-SLID)

**Post BeoL Via First TSV Technology**

<table>
<thead>
<tr>
<th>Technology name</th>
<th>Through Si Via Technology ICV-SLID</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Key characteristic</strong></td>
<td>TSVs for 5-100 µm thick silicon wafers</td>
</tr>
<tr>
<td></td>
<td>Via first concept</td>
</tr>
<tr>
<td></td>
<td>Post Backend-of-Line (use of fully fabricated devices)</td>
</tr>
<tr>
<td></td>
<td>Wafer scale process</td>
</tr>
<tr>
<td></td>
<td>Water-to-water and chip-to-water stacking (KGD)</td>
</tr>
<tr>
<td><strong>Devices to be stacked</strong></td>
<td>ICs and MEMS devices (wafers or bare dies)</td>
</tr>
<tr>
<td><strong>Form factor (±/0/±)</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Critical dimensions (density/die thickness) / number of layers/stand-off height)</strong></td>
<td>TSV hole dimension in silicon: 3 x 3 or 3 x 10 µm²</td>
</tr>
<tr>
<td></td>
<td>Via pitch TSVs: 10 µm</td>
</tr>
<tr>
<td></td>
<td>SLID pads: 30 x 30 µm², via pitch 60 µm (standard)</td>
</tr>
<tr>
<td></td>
<td>30 x 5 µm², 10 µm (high resolution)</td>
</tr>
<tr>
<td></td>
<td>Interconnect density: 10⁸-10¹⁰ mm⁻²</td>
</tr>
<tr>
<td></td>
<td>Stand-off height SLID layers: ~10 µm</td>
</tr>
<tr>
<td></td>
<td>Number of layers: 3 tested (in principle unlimited)</td>
</tr>
<tr>
<td><strong>Electrical parameters</strong></td>
<td>Resistance per interconnect: 350 mΩ (nongate, 3 x 10 x 50 µm) incl. SLID</td>
</tr>
<tr>
<td><strong>RF properties</strong></td>
<td>C=1 pF at 10 µm distance, C=0.5 pF at 150 µm distance</td>
</tr>
<tr>
<td><strong>Reliability / Yield / Maturity</strong></td>
<td>Simulation results: Regions of high stress and strain: the via itself (in case of Cu TSV), upper and lower end where the BEOL metal layers are connected (in case of W TSV)</td>
</tr>
<tr>
<td><strong>Road map (density) / future potential (2015) / feasibility</strong></td>
<td>Pitch reduction for TSVs to 3 µm (depth 20 µm) ~10⁸ mm⁻²</td>
</tr>
<tr>
<td><strong>Adaptability to new applications</strong></td>
<td>Flexible for applications (ASICS) available on wafer-level</td>
</tr>
<tr>
<td></td>
<td>Flexible TSV etch process sequence for typical IMD-layers and Si- and SiGe-layers, no constraints in physical layout; high density of vertical interconnects</td>
</tr>
<tr>
<td><strong>Cost of ownership / volume of production</strong></td>
<td>Most cost-effective for wafer-to-wafer stacking (for high yield and identical devices, e.g. memory stacks)</td>
</tr>
<tr>
<td></td>
<td>Most cost-effective for chip-to-wafer stacking with KGDs (for non-identical devices, e.g. heterogeneous systems)</td>
</tr>
<tr>
<td><strong>Manufacturing / Packaging</strong></td>
<td>Complete manufacturing in Wafer Fab or partly Wafer Fab (TSV) and Packaging House (stacking and SLID)</td>
</tr>
</tbody>
</table>

---

**Al**

---

**W-filled**

---

**Cu**

---

**Cu₃Sn**

---

**Cu**

---

**2 µm**

---

**Top-Chip (17 µm)**
Post Backend-of-Line TSV Process

Disadvantage 😞
BEOL intermetal-dielectrics have to be etched prior to silicon via etch

- For 3D Integration of various More than Moore products there is no cost-effective option
- Components are usually available as completely fabricated devices only
Post Backend-of-Line TSV Process

Disadvantage 😞

BEOL intermetal-dielectrics have to be etched prior to silicon via etch

- For 3D Integration of various More than Moore products there is no cost-effective option
- Components are usually available as completely fabricated devices only

TSV technology for automotive application (metallization of trenches by CVD tungsten)
Hollow Vias and Gold stud bump bonding (HoViGo)

TSV and interconnects for MEMS/ASIC

- TSVs for 300 - 1000 µm thick silicon wafers
  - Via first concept
  - TSV hole dimension in silicon: 20 x 50 or 50 x 50 µm²
    - Resistivity per TSV < 10 Ohm/via (300 µm wafer thickness)
  - **Min pitch TSVs: 110 µm** (rectangular) - 140 µm (square)
    - Corresponding TSV densities: ~ 5000 cm⁻²

- Interconnects compatible with inlets and released structures (MEMS)
  - Completely dry processing
  - Chip-to-wafer stacking
  - Min pitch Au stud bumps: 90 µm
    - Corresponding Au stud bump density: ~ 12000 cm⁻²
  - Stand-off height Au stud bumps: 10-15 µm
  - Number of layers: 2 tested (in principle unlimited)
Hollow through-silicon vias

Process:
- 300 µm thick 6" Si wafers
- 2.5 µm thermal SiO2
- Strip SiO2 on the backside
- Al sputter backside
- Lithography via holes frontside
- RIE SiO2 frontside
- DRIE using modified Bosch process
- Strip Al and SiO2
- 1 µm thermal SiO2
- 1 µm LPCVD polySi
- POCl3 doping of polySi
- Al sputter both sides
- Lithography both sides using dry-film resist
- RIE Al and polySi both sides

Alcatel AMS200
I-productivity
16 µm / min
(50 x 50 µm²)
Hollow through-silicon vias

TSVs for the TPMS sensor:

Requirements:
- Mechanical stability
- Electrical performance (< 30 Ohm / via)
- Reliability
  - Thermal cycling -40°C to +150°C
  - Post processing at 260°C (lead free soldering)
- Hermetic sealing
- High yield
- Low cost

Hollow TSVs:
- Suitable for thick wafers (300 – 1000 µm)
- Highly doped polysilicon
- No stress issues due to CTE mismatch (hollow)
- Allows post-processing up to 400°C
- Hermetic sealing by bonding (to be demonstrated)
- Simple process

Results technology demonstrator:
- Resistance: 7.5 Ohm / via
- Only failing dies at the wafer edges
- 98% yield on daisy chains with 80 vias
  (when excluding the dies at the wafer edge)
Interconnect for sensor and BAR

- Interconnect technology for stacking sensor and BAR onto the TX-µC stack:

  - Requirements:
    - Chip to wafer technology
    - Lead free
    - Electrical performance
    - Mechanical strength
    - Stand-off height < 30 µm
    - Reliability
      - Thermal cycling -40°C to +150°C
      - Post processing at 260°C (lead free soldering)
    - High yield
    - Low cost

  - Selected alternatives:
    - Au stud bump bonding (SBB)
      - Source: SINTEF
    - Cu/Sn solid-liquid interdiffusion (SLID)
      - Source: SINTEF / FhG IZM
Au stud bump bonding

- Process used for the TPMS demonstrator:
  - Au stud bumping on sensor & BAR wafers
    - Diameter +/- 50 µm
    - Height +/- 30 µm
  - Wafer dicing
  - Flip-chip bonding (chip-to-wafer)
    - Sensor (first) : with Epotek 353ND underfiller
    - BAR (last) : without underfiller
    - Thermocompression bonding
      - Bond force : 20 – 30 N for 10 s
      - Tool : 200 °C
      - Chuck : 120 – 140 °C
    - Thermosonic bonding
      - Bond force : 12 – 20 N for 2 s
      - Tool : room T
      - Chuck : 120 – 140 °C
Au stud bump bonding

- **Electrical results:**
  - Larger spread and bad reliability when the TX substrates had not been subjected to an O$_2$/H$_2$O plasma strip
  - Higher resistance in some cases, typically for bumps that were squeezed less (height > 15 µm)
  - Thermal cycling (-40°C to +150°C) and 30 min at 260°C has little impact on most of the devices that were subjected to the O$_2$/H$_2$O strip
Au stud bump bonding

Summary stud bump bonding results:

- Electrical resistance: 0.10 Ω per bump
- Shear strength: Sensor > 50 MPa, BAR ~ 27 MPa
- Thermal cycling: -40°C to +150°C and 30 min at 260°C stress have little effect
- Stand-off height: 8 - 15 µm

😊 No wet processing involved
😊 No need for UBM or passivation layers
😊 Serial process: most cost-effective for stacking devices with lower I/O counts

Source: SINTEF
Cu/Sn Solid-Liquid Interdiffusion

- Process SLID technology demonstrator:
  - Preparation of dummy sensor and ASIC wafers:
    - 10 x 10 µm² contact openings on bondpads
    - electroplated Cu bumps ASIC side: 50 µm Ø (circular)
    - electroplated Cu/Sn bumps sensor side: 40 µm Ø (circular)
  - Dicing of sensor wafer
  - Mounting sensor chips on handle wafer
  - Wafer-to-wafer bonding: 3 kN, 325°C, EVG bonder
Cu/Sn Solid-Liquid Interdiffusion

Process:
- During bonding at 325°C, Sn melts
- Cu diffuses into the melted Sn layer to form Cu₆Sn₅ (η)
  → the compound solidifies and the stack is fixed
- Cu₆Sn₅ (η) then transforms into the thermodynamically stable Cu₃Sn (ε) phase with melting point > 600°C

Cross-sections and SEM-EDS analysis:
- Nearly all Sn has reacted with Cu to formed the stable Cu₃Sn (ε) phase
- On some samples (2 out of 12) a small area with Cu₆Sn₅ (η) remains
- After thermal cycling (-40°C to +150°C) no areas with Cu₆Sn₅ (η) were seen anymore
- Otherwise, no changes were observed after thermal cycling and 30 min at 260°C
- 10 µm misalignment

Source: SINTEF / FhG IZM

Melting temperatures
- Sn: 232°C
- Cu: 1083°C
- Cu₆Sn₅ (η): 415°C
- Cu₃Sn (ε): 670°C
Cu/Sn Solid-Liquid Interdiffusion

Summary SLID results:

- Electrical resistance: very low (measurement dominated by Al conductors)
- Shear strength: ~ 37 MPa
- Thermal cycling - 40°C to +150°C and 30 min at 260°C stress have little effect
- Stand-off height: ~ 8 µm

😊 Suitable for high I/O counts
😊 Scalable to pitch < 50 µm (limited by bonder alignment accuracy)
😊 Wet processing required (e.g. inlets would need to be protected)

Source: SINTEF
TPMS demonstrator results

- Successful measurements on PCB level:
  - Communication with TX is working
  - Communication with μC is working
    - μC – TX (SnAg μ-bumps)
    - TX TSVs (W-TSVs)
  - BAR is running at correct frequency
    - TX-BAR interconnect (Au stud bumps)

- Sensor performance to be measured soon

MEMS / TX / μC 3D stack
- Source: SINTEF

Micro-PCB
- Source: Infineon Technologies

Molded Interconnect Device (MID) with integrated loop-antenna

Miniaturized TPMS ~ 1 cm³
Acknowledgements

This report is partly based on the e-CUBES project which is supported by the European Commission.

Colleagues of the e-CUBES project, especially
- Werner Weber, Thomas Herndl and Josef Prainsack, Infineon Technologies
- Timo Seppänen, SensoNor
- Lars Nebrich and Robert Wieland, Fraunhofer IZM-Munich
- Jürgen Wolf and Matthias Klein, Fraunhofer IZM-Berlin
- Thor Bakke and Lars Geir Whist Tvedt, SINTEF

Vincent McTaggart, Kulicke and Soffa Industrial (KNS)
- For providing the bumping service

Gerhard Hillmann, Datacon Technology GmbH
- For providing the chip to wafer bonding service and process development