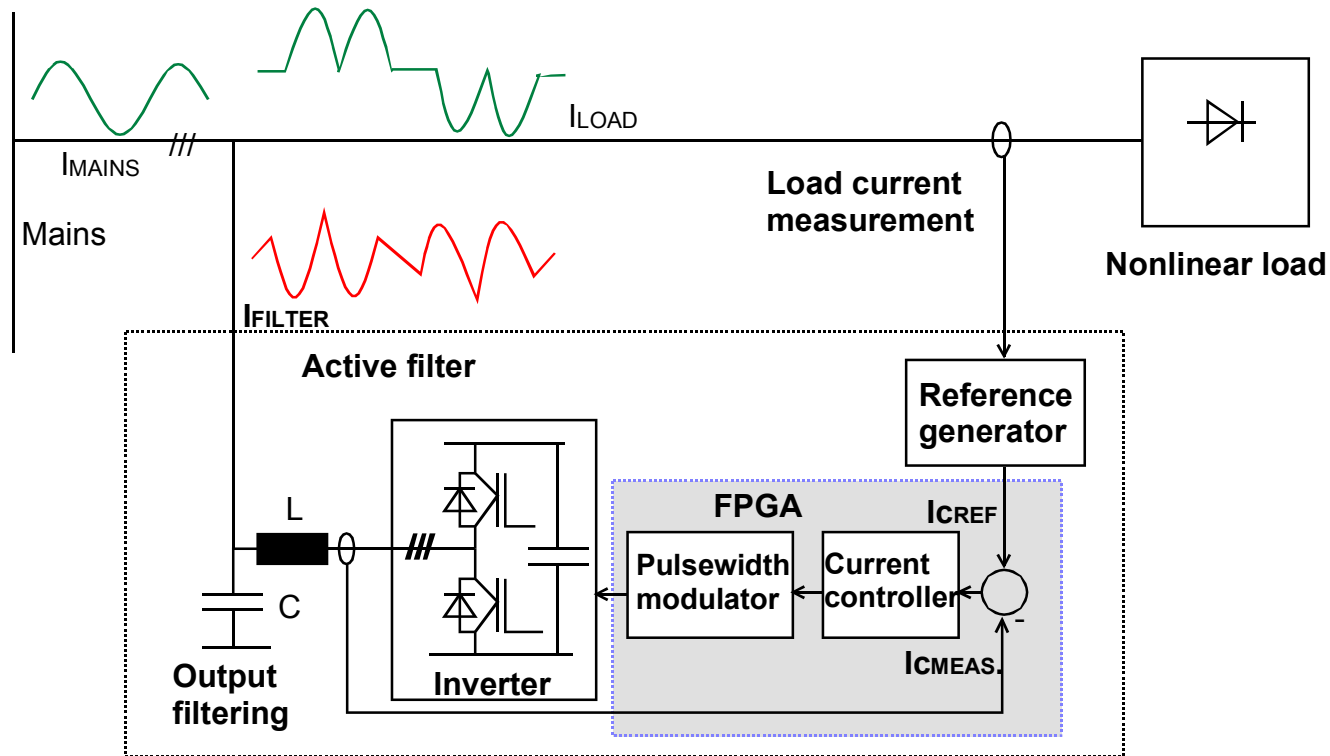


Paper presented at EPE 2003

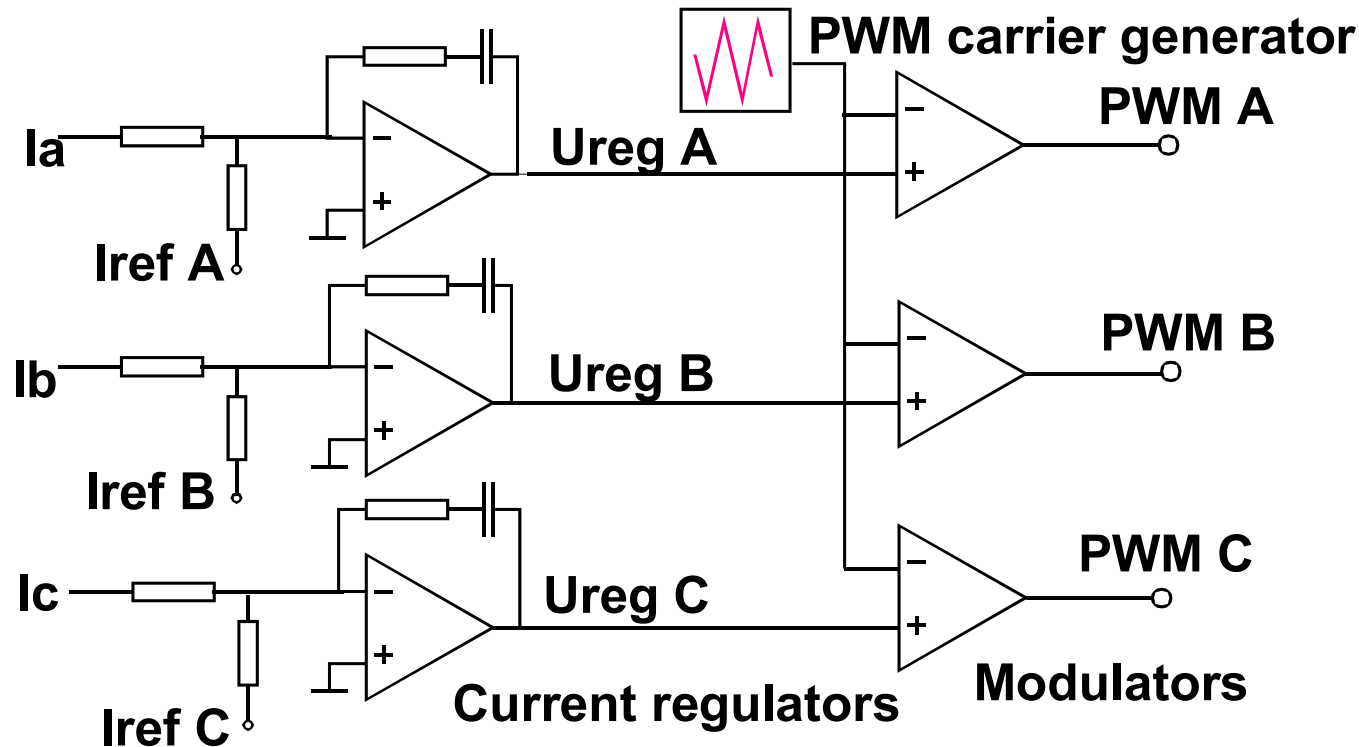
FPGA based digital current controllers

Example case: Active shunt filter.



- Non-linear loads draw distorted current from the mains
- Active filter injects currents that cancels distortion.

Analogue current controller

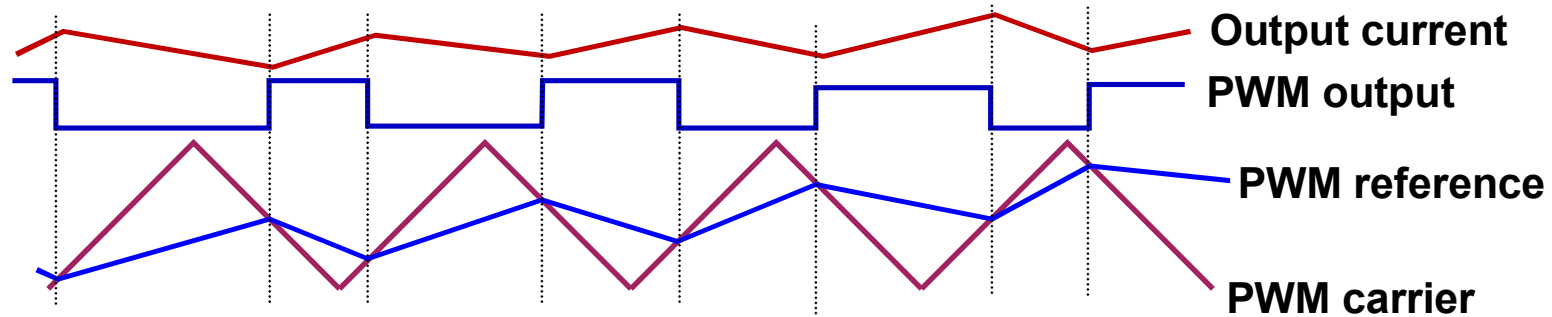


- Analogue circuits works continuously
- Allows high gain, giving good performance.

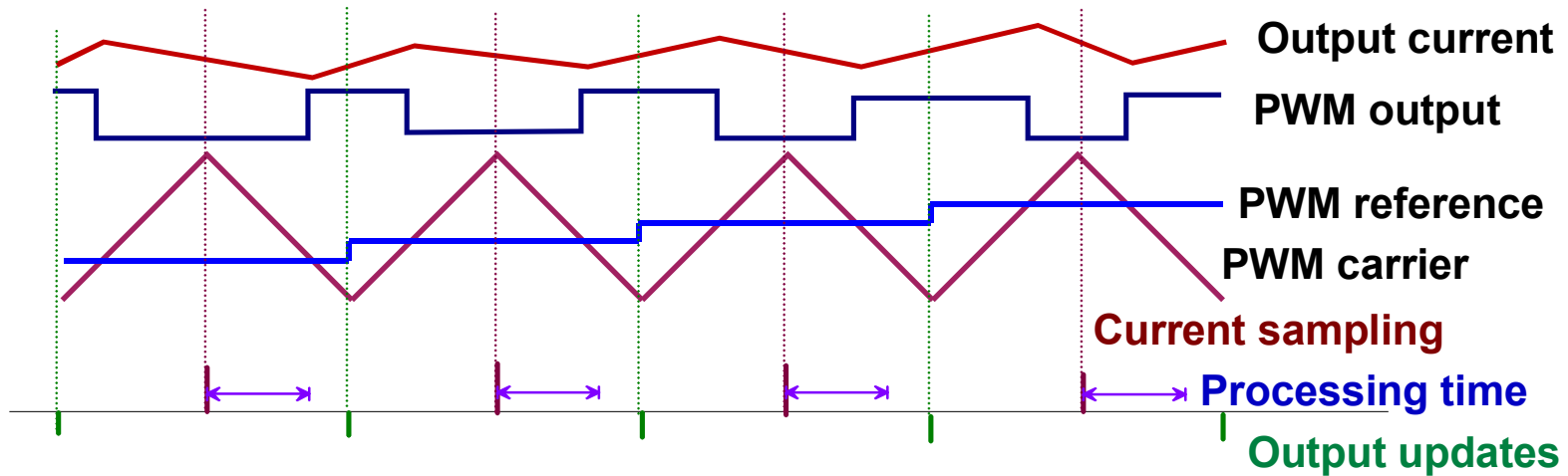
Design target

- **Digital uP/DSP' based controllers has inferior performance compared to analogue controllers due to delay introduced by sampling.**
- **The challenge: To make a digital control system that is fast enough to give almost continuous signal processing, similar to an analogue circuit.**
- **Our approach: Use a FPGA based parallel signal processing system, with data rates much higher than the switching frequency, to obtain almost continuous signal processing.**

Signal delay

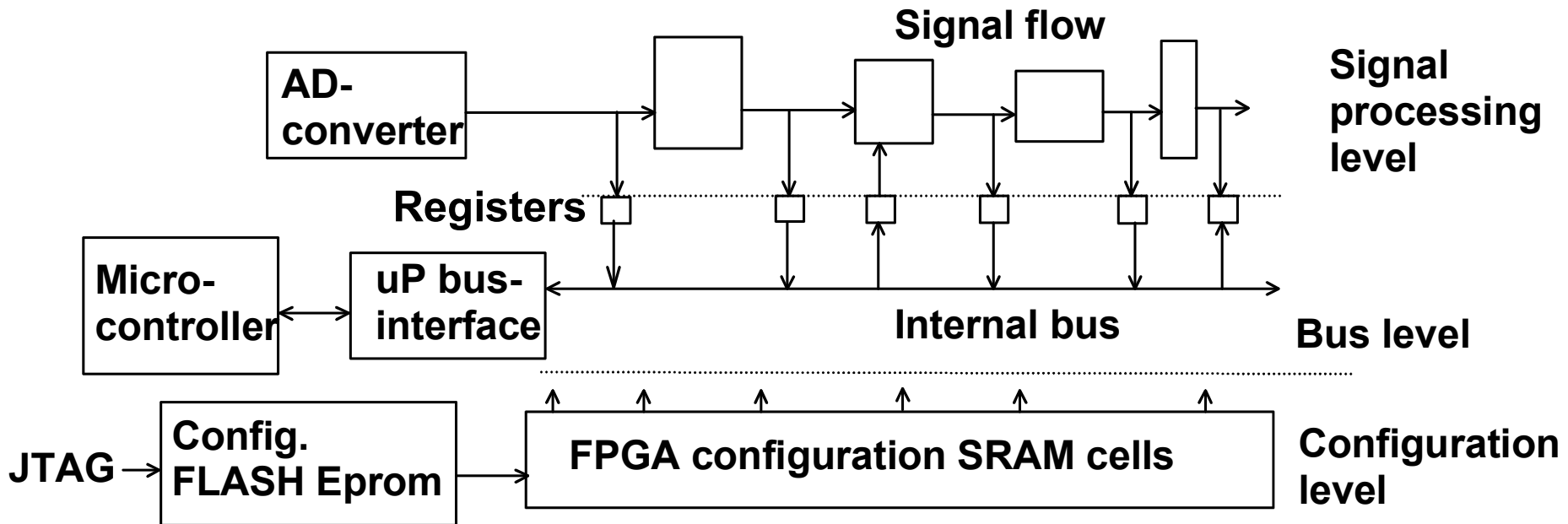


Analogue current controllers



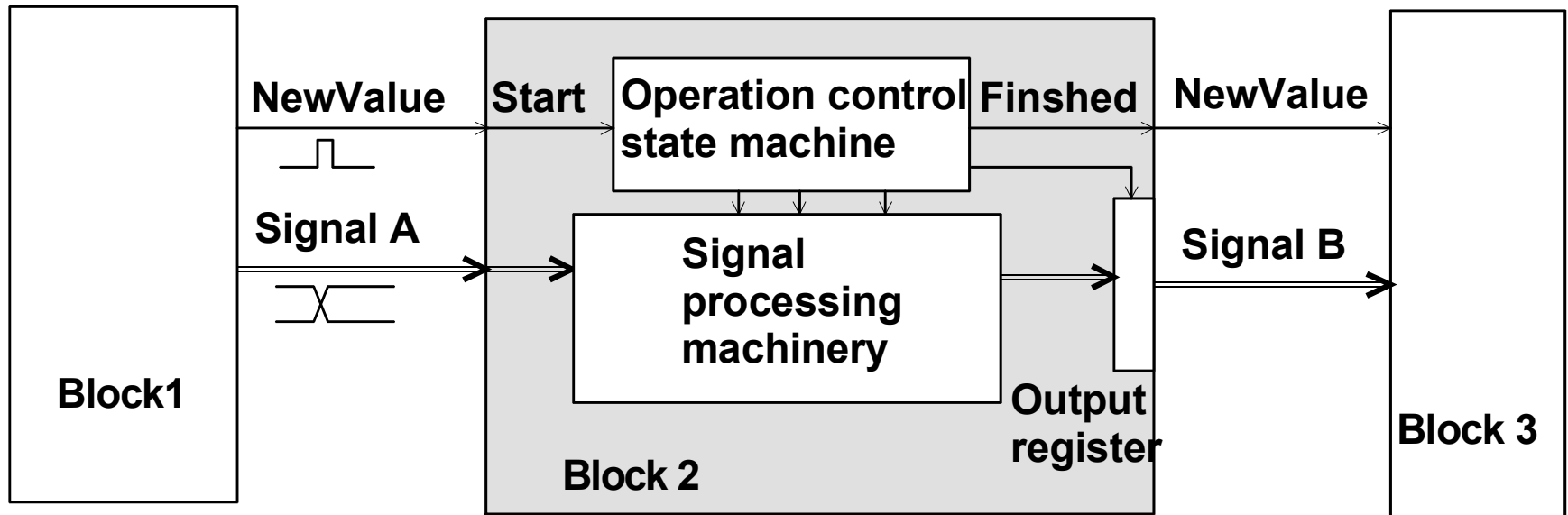
DSP based digital controllers

FPGA design structure



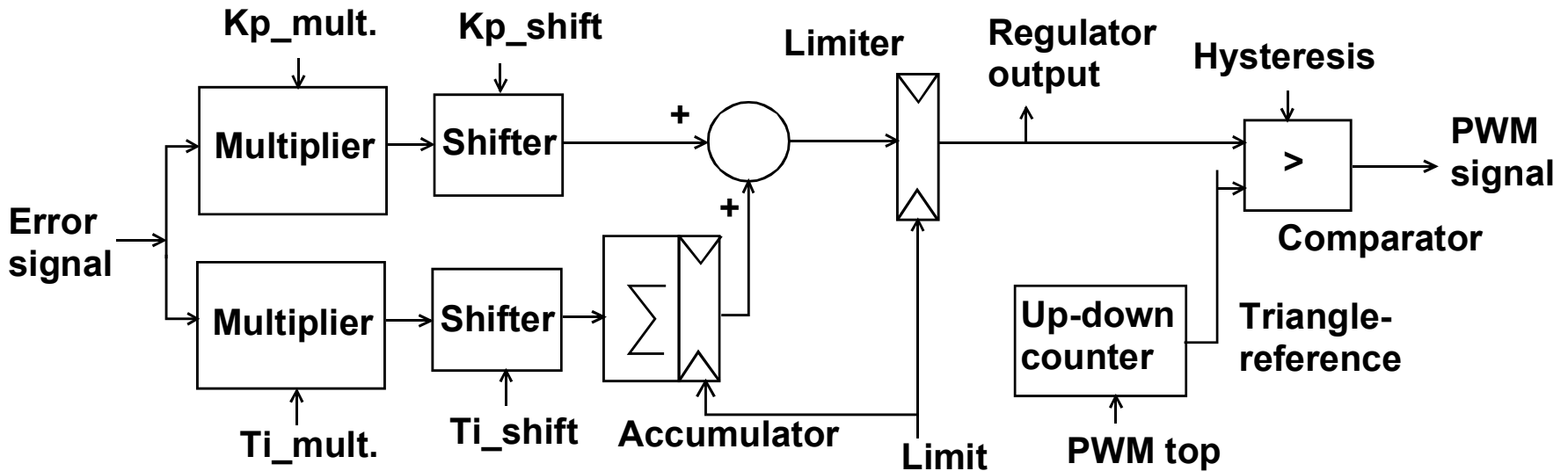
- Several processing blocks in the signal processing chain.
- AD converter drives the signal flow. Updates values every 0,67ms.
- Signals inside the FPGA are available on the processor data bus.

Signal flow between blocks



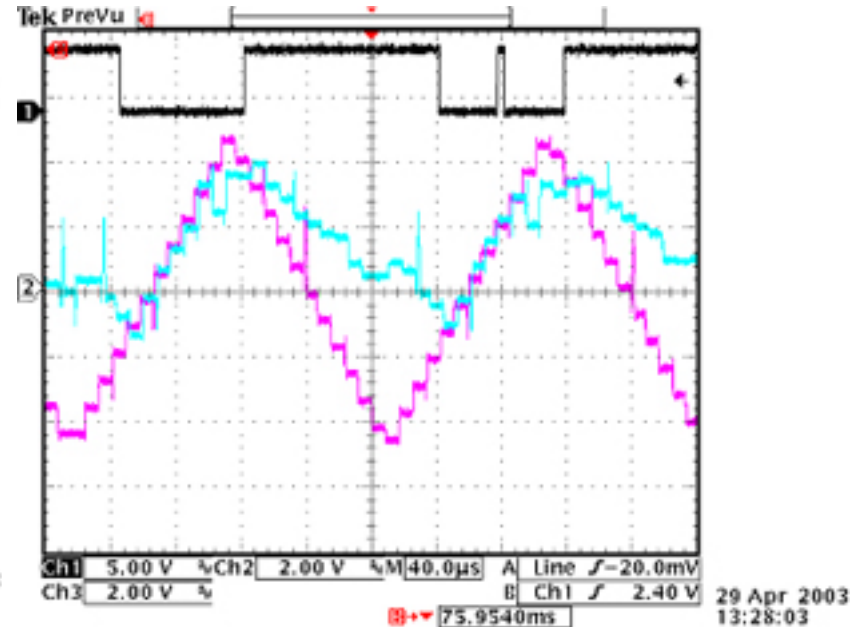
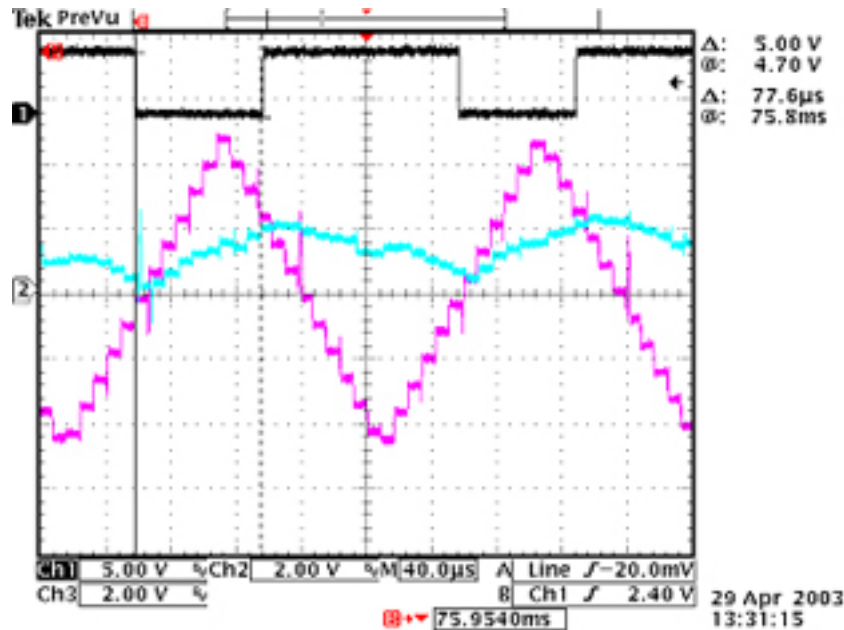
- A new processing sequence triggered by a NewValue flag
- When finished, outputs are updated, and NewValue flag pulsed.
- The block enters idling state, while the next block starts processing.

PI controller



- Two stage signal scaling: multiplier and a shifter.
- An accumulator performs integration.
- Limiters on accumulator and the output signal.
- Modulator consists of a up-down counter and comparators.

Pulse modulator.



Normal gain.

Too high gain. Extra pulses.

PWM output signal (black), Controller output signal (blue), Modulator carrier wave (pink).

Switching frequency: 10 kHz.

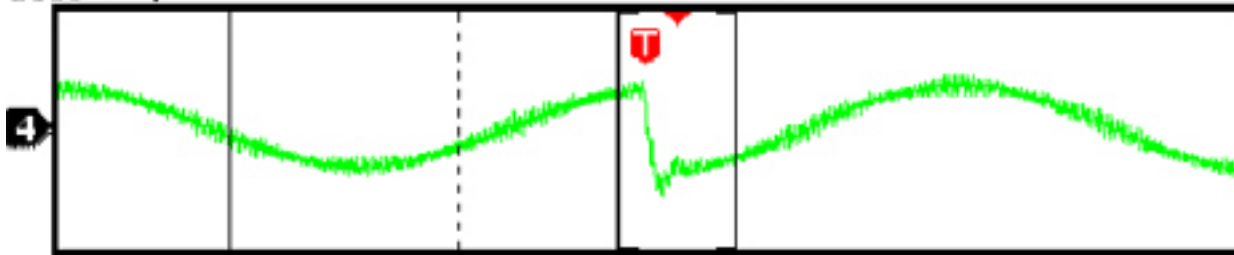
Sampling rate: 1,5 MHz.

Note: DA-converter running at 8 μs update rate causes steps and glitches.

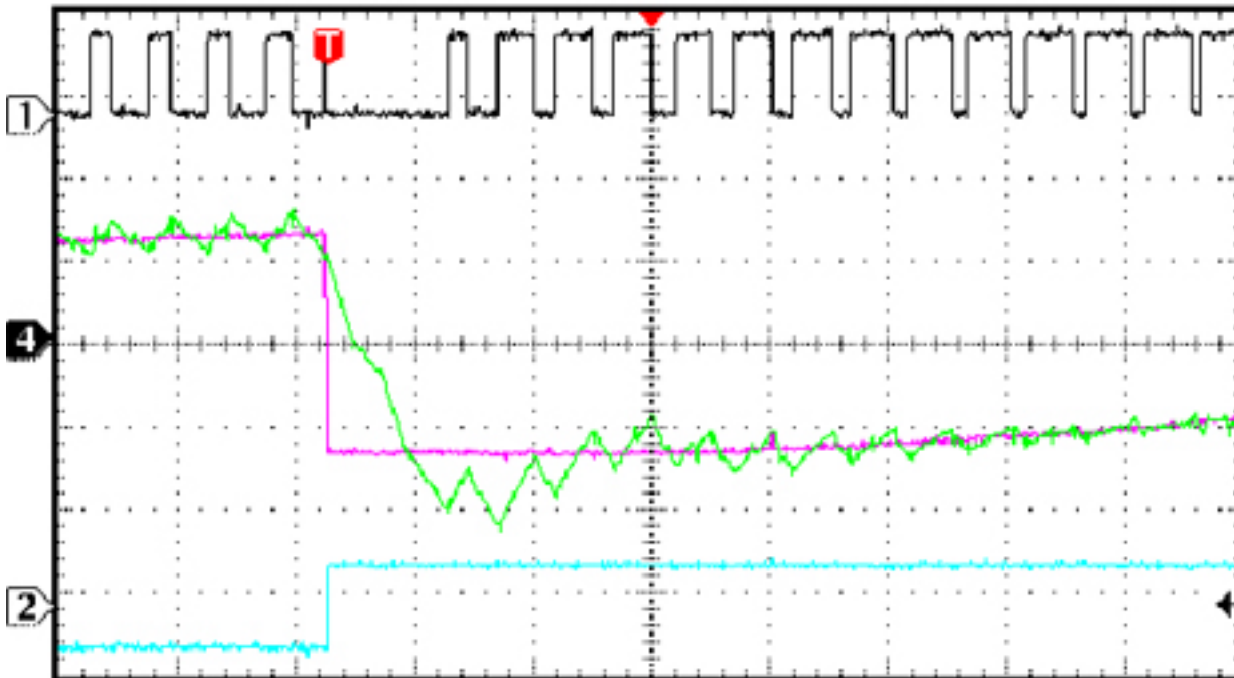
Step reversal of reactive current reference

Tek Stop

M4.00ms



Δ : 100mV
 $@$: -44.0mV
 Δ : 7.76ms
 $@$: -14.1ms



PWM signal

Reactive current reference

Phase current reference

Measured current [20A/div]

Ch1 5.00 V B_V Ch2 2.00 V B_V Z 400µs A Ch2 \int 80.0mV
 Ch3 750mV B_V Ch4 200mV B_V

1.08800ms

29 Apr 2003
14:14:12



Experiences

- **The FPGA based digital system behaves as its analog counterpart.**
- **FPGA based parallel signal processing allows very high data rates.**
- **Using a FPGA gives immense flexibility.**
- **Many other circuit variants and extensions are possible.**
- **AD converter speed and noise may in some applications limit achievable performance.**
- **Development work in VHDL for a FPGA is substantially heavier than doing a similar job in C for a microcontroller.**