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PROJECT MEMO

MEMO CONCERNS

Adaptation and testing of a Phase-Locked Loop method

DISTRIBUTION

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A Phase-Locked Loop (PLL) is a device that makes one signal to follow another one in frequency as well as phase. When a Voltage Source Converter (VSC) is interfaced directly to an AC-network with its AC-side (active front end, STATCOM, PLC, active filter, etc), the control system of the VSC needs a synchronized reference vector as basis for its internal control loop.

This report investigates a PLL-method based on a widely used principal to produce a pure sinusoidal 3-phase output signal, phase-looked to a 3-phase input quantity of the network, e.g. the phase voltages. The basic topology consists of a voltage-controlled oscillator (VCO), a low-pass filter, a PI-regulator and a phase shift meter. The key component is the phase shift meter, which is set up to produce a DC-output for a positive sequence phase shift, and AC-components for all other quantities, including negative sequence components of the input.

The report shows a simplified algorithm for realising the phase shift meter, at least when comparing to what we know from the algorithm implemented in the “Phase Difference” component of the simulation program PSCAD/EMTDC.

The PLL-loop is thoroughly tested by simulations in PSCAD/EMTDC, by applying input signals emulating phase voltages of the AC-network, with varying deterioration (harmonics, dissymmetry, etc).

The final PLL-model makes a basis for the implementation in the control system (micro-controller) of a 20 kW VSC-prototype. The implementation is reported in Project Memo AN 00.12.39.

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