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229196

Project acronym:
piezoVolume

Project full title:
High volume piezoelectric thin film production process for microsystems

Collaborative Project targeted to a special group (such as SMEs)
Grant Agreement No.:

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D 3.5
Device prototypes, generation 2

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential , only for members of the consortium (including the Commission Services)	

Deliverable number:	D 3.5
Deliverable name:	Device prototypes, generation 2
Work package:	WP3 Design and fabrication of device prototypes
Lead contractor:	SIN

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Abstract

Device prototypes with of all device types and planned processing routes have been delivered to the application partners. The Generation 2 devices have slight modifications in the design compared to Generation 1. The device prototypes will be characterized and tested in related work packages together with Generation 1 devices.

Public introduction[1]

Device prototypes of all device types and planned processing routes have been delivered to the application partners. The Generation 2 devices have slight modifications in the design compared to Generation 1.

[1] According to Deliverables list in Annex I, all restricted (RE) deliverables will contain an introduction that will be made public through the project WEBsite (www.piezovolume.com)

TABLE OF CONTENTS

Page

1 BACKGROUND AND SUMMARY 4
2 PROCESSING ROUTES 5
2.1 Process route A 5
2.2 Process route B 5
2.3 Process route C 5
3 DEVICES DELIVERED TO OCÉ 6
3.1 Test devices on wafer 6
4 DEVICES DELIVERED TO VERMON 7
5 DEVICES DELIVERED TO SONITOR 8
6 DEVICES DEILVERED TO AIXACCT 10

1 BACKGROUND AND SUMMARY

The background for the delivered MEMS devices is described in the previous deliverable D3.2 *Designs* and D1.4 *Report on integration, design and fabrication rules*

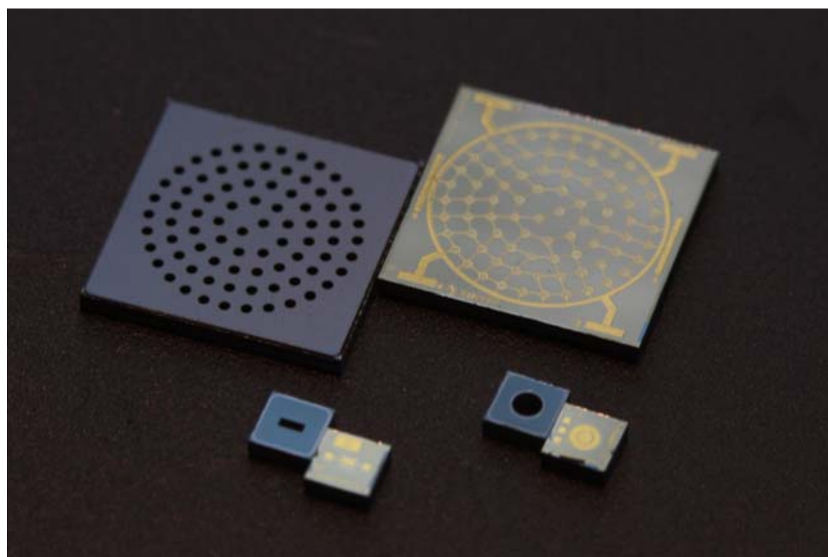

Figure 1-1: Presentation quality picture of piezoVolume-devices

The image above (Figure 1-1) shows examples of the devices as delivered. More presentation style images will become available on the project web-site and for other uses as required by the project partners. The Generation 2 devices have slight modifications in the design compared to Generation 1.

2 PROCESSING ROUTES

For reference, a short description of the processing routes is given here, as introduced previously in D1.4 *Report on integration, design and fabrication rules*.

For details of the actual processing (step-by-step journal) of each wafer, the project partners may refer to the SINTEF internal documentation reference "PF 12-028". This documentation is certified according to ISO 9001:2008.

2.1 Process route A

Process A (For sensor-type devices with inter-digital-electrodes). Without a bottom electrode, but with an additional thin oxide layer deposited on the substrate stack prior to deposition of the functional piezoelectric thin film layer.

2.2 Process route B

Process B (For sensor-actuator type devices). The proven processing route (similar to that used in previous projects) and know-how of SINTEF and EPFL prior to the project. The process is based on a platinum bottom electrode deposited on the silicon substrate prior to deposition of the functional piezoelectric thin film layer.

2.3 Process route C

Process C (For sensor-actuator type devices with additional metal routing layer). As process route B, with an additional metal routing layer on an additional polymer based dielectric layer on the top electrode.

3 DEVICES DELIVERED TO OCÉ

See D3.2 *Designs* for details on the device designs.

As requested after Generation 1 tests, arrays on a single, larger wafer piece of typically 10x10 devices are preferable for testing at Océ.The piezoVolume design types for Océ having been processed as type B and C respectively-were shipped as the devices were finished. The main process variant (type C) as specified include the extra dielectric layer for routing and bonding pads also using the (extra) top metal layer. The chips have two pads each: one for the top electrode and one for the bottom electrode and have the design version (A, AA, B, BB, C, CC) and position on the wafer marked separately. The dies/chips were visually checked, but not closely inspected or tested prior to shipment.

3.1 Test devices on wafer

The test devices (as described under "test devices") will be tested together with project partners for process documentation and for generating improved process data for the modelling tools

Table 3.1: Devices delivered to Océ

Device Type	# Devices	Wafer ID and [process type]	Delivery Date
Actuator-test-devices	NA	pV210, process type C	2012-07-06
Actuator-test-devices	NA	pV202, process type B	2012-07-06

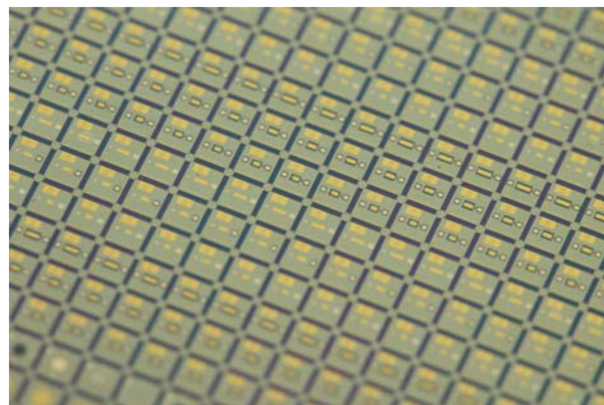

Figure 3-1: Picture of Océ device from wafer pV210 (type C)

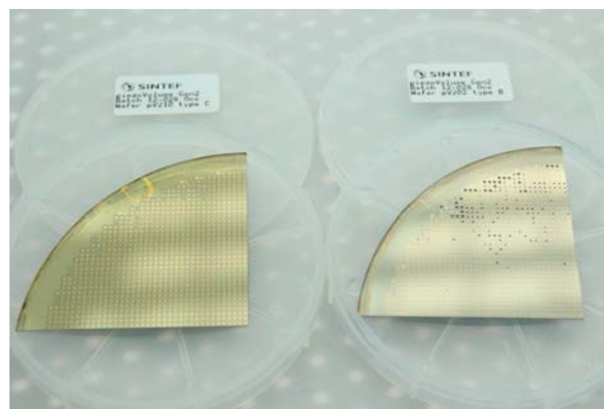

Figure 3-2: Arrays of devices for Océ as delivered. Left: Wafer pV210 (type C), Right: Wafer pV202 (type B), with some damaged devices, membranes.

4 DEVICES DELIVERED TO VERMON

See D3.2 *Designs* for details on the device designs.

Compared to Generation 1, the nominal membrane size is somewhat reduced in Generation 2. The design-types made with process B include types with two types of connecting routing lines – one with the thin gold of the first metallization and one with the thicker gold of the second metallization. The design types for process C (extra routing layer on dielectric) have also been made and shipped. A few dies have been picked off for electrical tests at SINTEF. These dies have not yet been inspected or tested.

Though we have made extra effort to avoid processing errors, and sort out obvious bad dies, a few shipped devices may prove to have processing damage, e.g. broken conductor lines, residue from polymer layers or similar. Bad devices may be used for packaging tests etc, or they may be discarded.

Table 4.1: Devices delivered to Vermon

Device Type	# Devices	Wafer ID and [process type]	Delivery Date
pMUT-devices	13	pV202, process type B	2012-07-06
pMUT-devices	9	pV210, process type C	2012-07-06

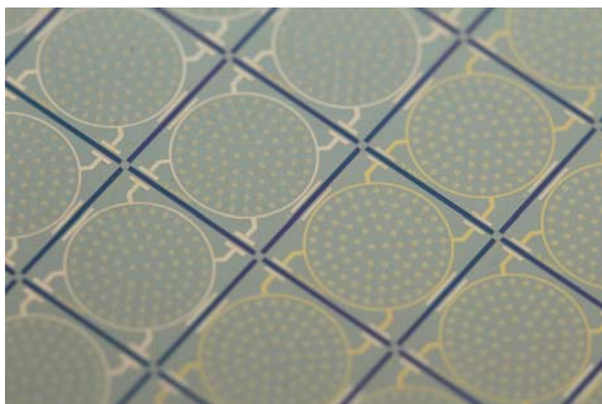

Figure 4-1: Image of Vermon devices on wafer, showing metal routing under and over polymer layer respectively, wafer pV210 (type C).

Figure 4-2: Generation 2 devices as delivered in Gel-Paks to Vermon. Left: 13 devices from process type B, Right: 12 devices from process type C (only 9 delivered)

5 DEVICES DELIVERED TO SONITOR

See D3.2 *Designs* for details on the device designs.

Two wafer diced (1/4) parts with microphone type devices are delivered on tape. The devices are marked type AA, BB and CC, having nominal membrane diameters of X-60µm, X and X+60µm. Sonitor will pick up the deliveries from SIN in person, pick off devices from tape as needed, and proceed to package (wire-bond etc.) and test the devices in cooperation with SIN and project partners. A few dies have been picked off for electrical tests at SINTEF. These dies have not yet been inspected or tested.

Table 5.1: Devices delivered to Sonitor (delivery dates are only indicative, as reported)

Device Type	# Devices	Wafer ID and [process type]	Delivery Date
Sensor-test-devices	NA	pV222 process type A	TBD
Sensor-test-devices	NA	pV202 process type B	TBD

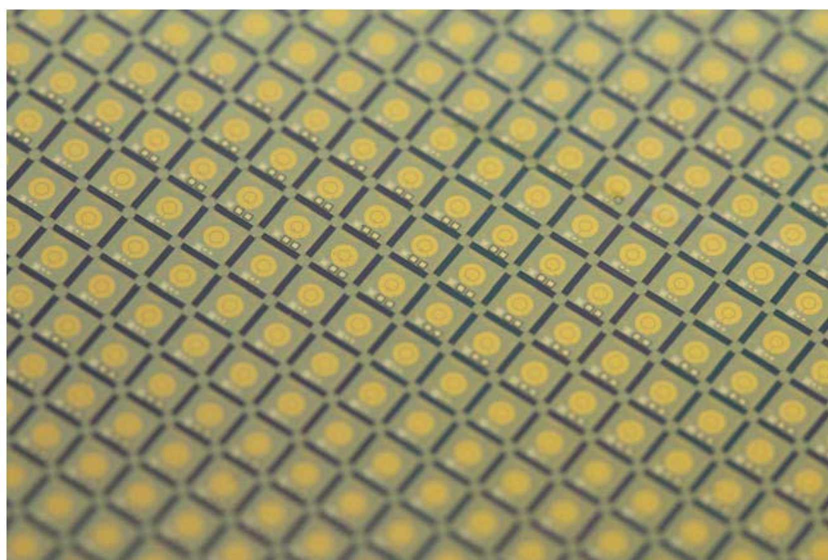

Figure 5-1: Sonitor devices from Generation 2

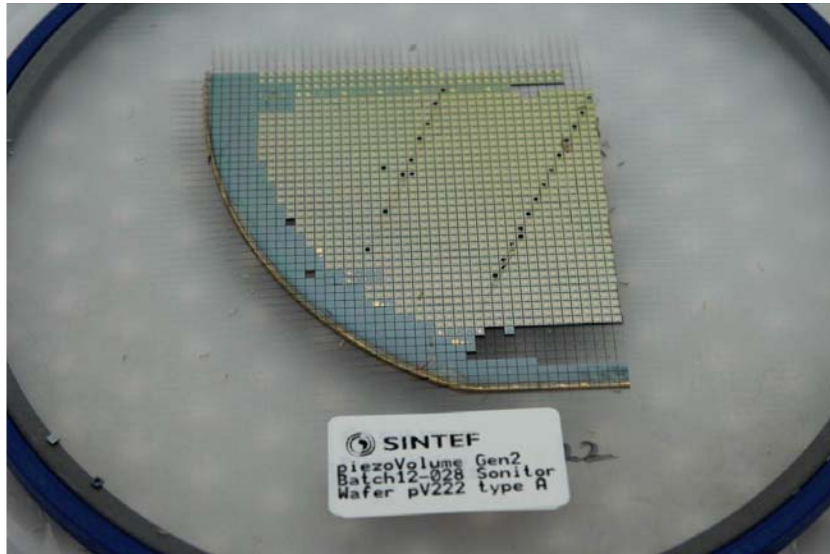

Figure 5-2: Generation 2 devices with process A for Sonitor on tape

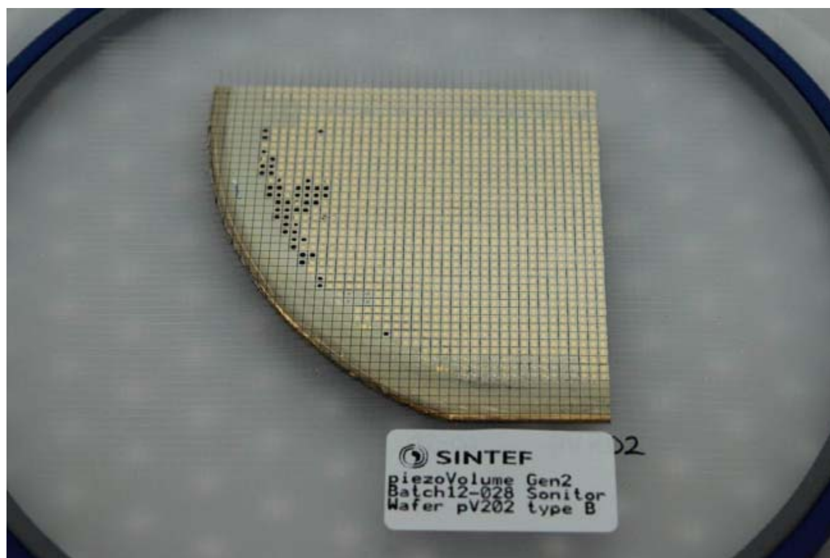

Figure 5-3: Generation 2 devices with process B for Sonitor on tape. Black devices are due to damaged membranes that did not survive the final processing steps.

6 DEVICES DEILVERED TO AIXACCT

One full wafer pV214, processed as complete wafer with process type B wafer as SINTEF batch PF 12-028 delivered in wafer box, see picture below. For testing on wafer level.

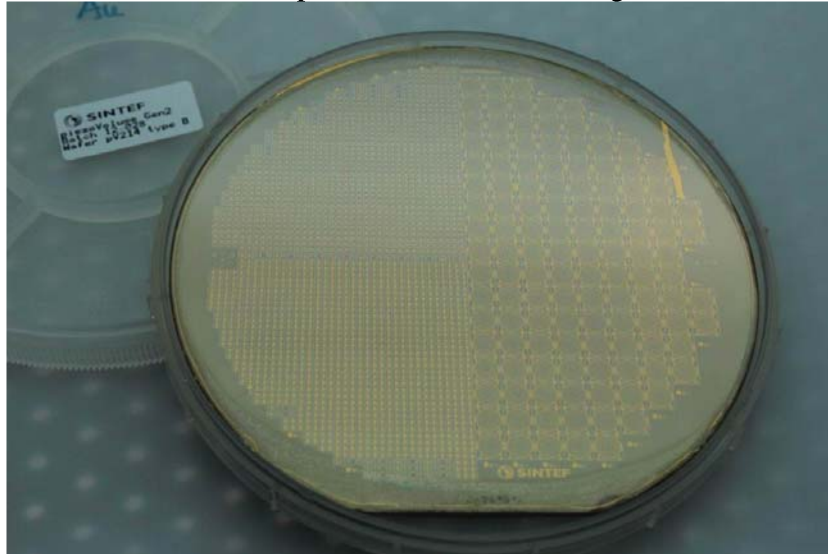

Figure 6-1: 1 full wafer pV214, processed as complete wafer with process type B wafer as SIN batch PF 12-028 as delivered in wafer box