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Abstract

This is the final version presenting the process steps and sequences needed to fabricate devices including piezoelectric thin films based on lead zirconate titanate (PZT) using the piezoVolume process. This documentation gives an overview and short introduction to the establishment of the fabrication processes specific to piezoMEMS at other suitable fabrication facilities (fabs).

Public introduction[1]

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[1] According to Deliverables list in Annex I, all restricted (RE) deliverables will contain an introduction that will be made public through the project WEBsite

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1 BACKGROUND AND MOTIVATION

The aim of the document is to present the process steps and sequences needed to fabricate devices including piezoelectric thin films based on lead zirconate titanate (PZT) using the piezoVolume process. The documentation gives an overview and short introduction to the establishment of the fabrication processes specific to piezoMEMS at other suitable fabrication facilities (fabs).

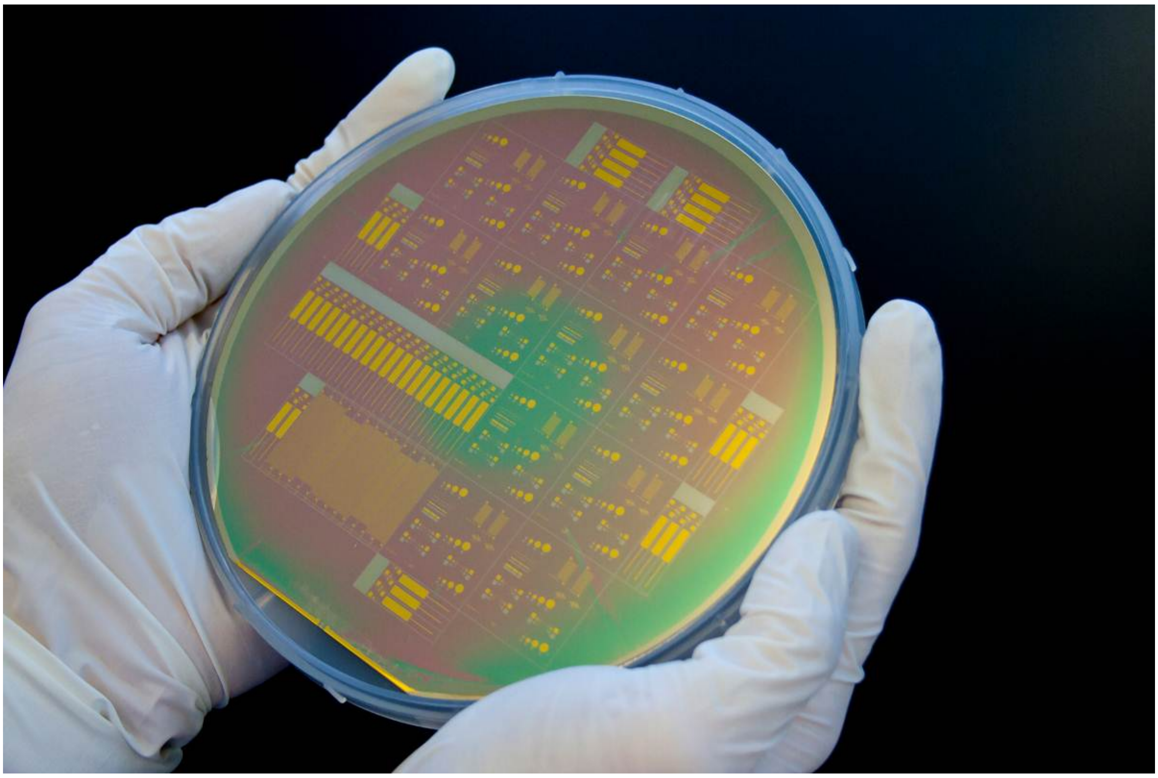

Figure 1.1: Wafer with piezoVolume test structures

The reliable integration of piezoelectric thin films into MEMS is a key enabling technology for a wide range of future products. Examples include ultrasonic imaging transducers, pressure and flow sensors, accelerometers, acoustic wave devices, energy converters, micromotors, micropumps, and microsensors for chemical analysis. Piezoelectric materials allow energy conversion between the electrical and mechanical domain. This conversion is shown in the schematic in Figure 1.2. The conversion from the mechanical to the electrical domain (i.e. a mechanical signal that yields an electrical signal) is defined as the direct effect, the conversion from the electrical to mechanical domain (i.e. actuation) is called converse effect. Several sensor structures utilise both effects at the same time.

Figure 1.2: The converse and direct piezoelectric effect.

There are several material systems of piezoelectric materials available. The two alternatives that are currently most interesting for MEMS applications are aluminium nitride and PZT. AlN is suitable for high frequency application and sensing due to its low dielectric constant, whereas PZT is suitable for low frequency operation < 500 MHz and for actuation due to its high piezoelectric constants.

While piezoelectric aluminium nitride (AlN) can be deposited in a CMOS compatible sputter process that is easy to industrialize, the deposition techniques for PZT ($Pb(Zr,Ti)O_3$) are far behind in maturity. However, PZT has an electromechanical coupling that is approximately 10 times higher and this has been our main motivation for developing this technology, and to take the technology to full production capability.

Applications can be:

- Ultrasonic imaging transducers
- Positioning systems
- Pressure and flow sensors (e.g. disposable blood pressure sensors)
- Gas sensors
- Energy harvester
- Accelerometers (e.g. for airbag deployment in collisions)
- Micropumps

2 INTEGRATION

Designs, process integration and fabrication procedures are closely interrelated. The piezoVolume process/fabrication chain is shown in the figure below:

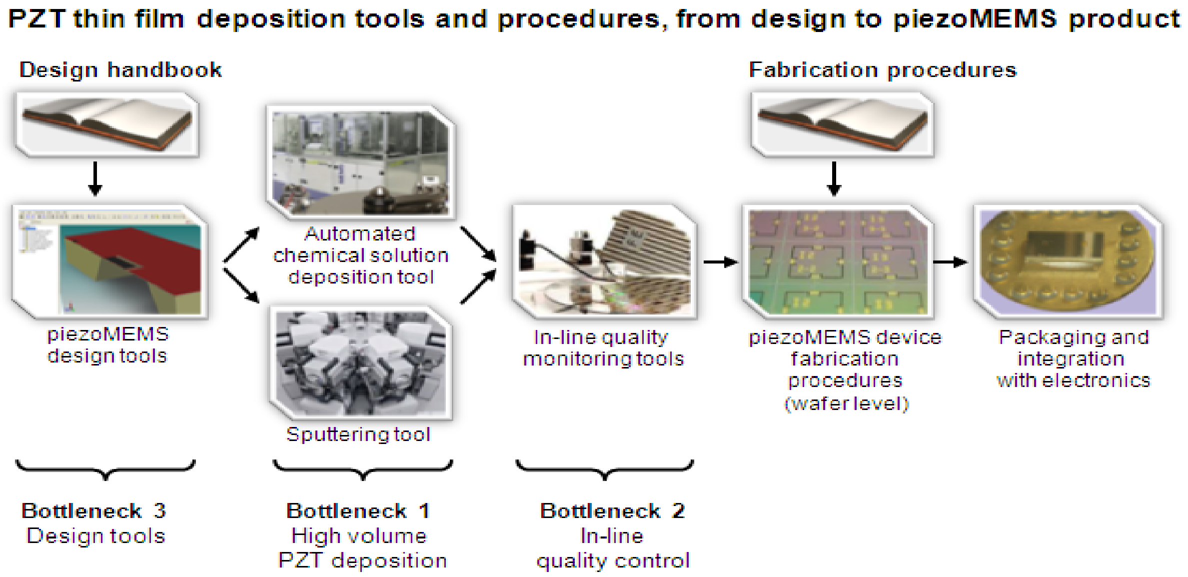

Figure 2.1: The piezoVolume process chain, from design to wafer level piezoMEMS device. Previous "bottlenecks" are shown.

2.1 PZT deposited with CSD

2.1.1 CSD PZT

CSD PZT provides high quality PZT thin films with a high transversal piezoelectric coefficient, $e_{31,f}$ around -14 C/m^2. Depending on the precursor solution chemistry PZT films with thicknesses up to several microns can be deposited on 100 mm and 150 mm (4” and 6” diameter) wafers. The piezoVolume project also aims to qualify the process for 200 mm wafers, the subject of on-going work.

A cross section of a PZT thin film is shown in Figure 2.2. Here eight sequential crystallizations performed during the CSD process of PZT are clearly visible. For high volume production, the effort has been to automate and speed up the layer-by-layer deposition process.

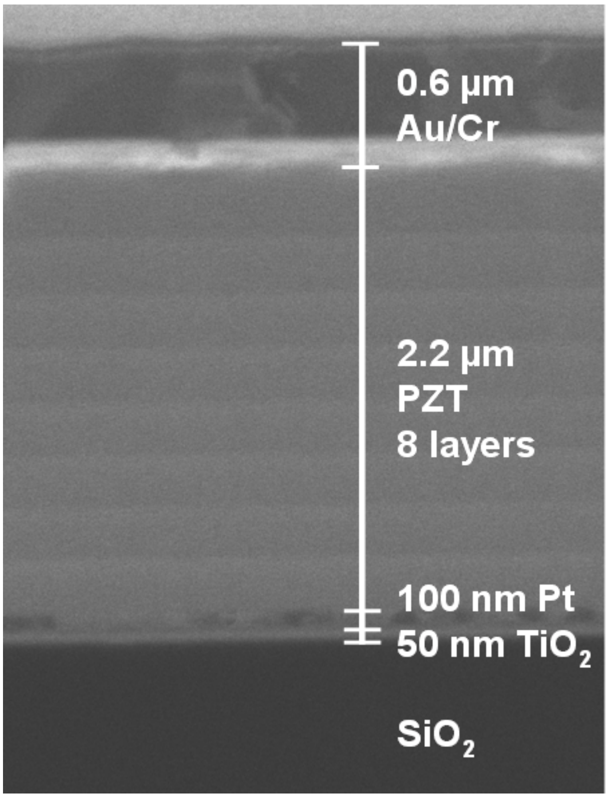

Figure 2.2: SEM image of a multimorph cross section milled by focused ion beam (FEI Company, The Netherlands).

2.1.2 Automated coating system for CSD

The coating system for CSD from Solar-Semi is based on an automated microcluster. Based on existing experience with spin-coaters, this high volume automation-line will be equipped with the following modules:

2 pcs.	Spin-coating-modules including solution supply
2 pcs.	Hotplates (for pyrolysis) / 2 pcs. Cool-plates
2 pcs.	RTP units (for crystallization) (RTP = Rapid Thermal Processing)
1 pc.	Handling system

Figure 2.3: Automated cluster tool

2.1.3 Performance

Using CSD it is possible to deposit high quality piezoelectric PZT films with a transversal piezoelectric coefficient $-e_{31,f}$ of 14-15 C/m^2 . The maximum thickness is ~4 µm.

Depending on the deposition tool and the amount of parallel processing which is implemented this method satisfies the throughput goal of 3,6 wafers/h*µm.

2.1.4 Integration

To integrate a CSD-cluster-tool into a wafer-fab, the following basic facility requirements should be available:

System dimensions	~ 3000 x 1500 x 2500 (W x D x H (mm))
System power supply:	3 x 400/230 VAC 50/60 Hz L1, L2, L3, N and PE
Power consumption:	Typically about 11 kW (without RTP)
Compressed air for pneumatics:	8 ± 2 bar, 5 µm filtered, dry, oil free
Vacuum for chuck and hotplate:	0.2 ± 0.1 bar
Nitrogen for tank-system, hotplate, RTP, etc.:	4.0 ± 0.5 bar
Oxygen for RTPs:	4.0 ± 0.5 bar
Different separate exhausts:	RTP/process/e-cabinet/hotplate/…

2.2 Sputtered PZT

Sputtering is a well known deposition technology providing high quality films for mass production at reasonable cost of ownership. The applications range from single metallic layer deposition of e.g. a reflective layer in optical storage technology to complex layer structures required e.g. for the magnetic storage or for devices in the semiconductor industry.
Fields of application for sputtering within the semiconductor business are e.g.

- Backside metallization
- Advanced packaging
- Solid state Lighting (LED)
- MEMS
- Antireflective coatings and waveguides
- BAW / SAW piezoelectric films, e.g. AlN
- Thin film read/write heads (magnetic storage)

2.2.1 Sputter tool for PZT

To get the best possible sputtered PZT, the perovskite phase has to be grown directly at a substrate temperature of about 600°C. The major obstacle to realize this process is that normal heater chucks in sputter equipment are not able to reach such temperatures. Therefore the standard hot chuck has to be exchanged by a so called very hot chuck where the heating of the chuck is done with a resistive coaxial heater with a maximum power of 2 kW and two control circuits to balance the heating at inner and outer diameter (Figure 2.4).

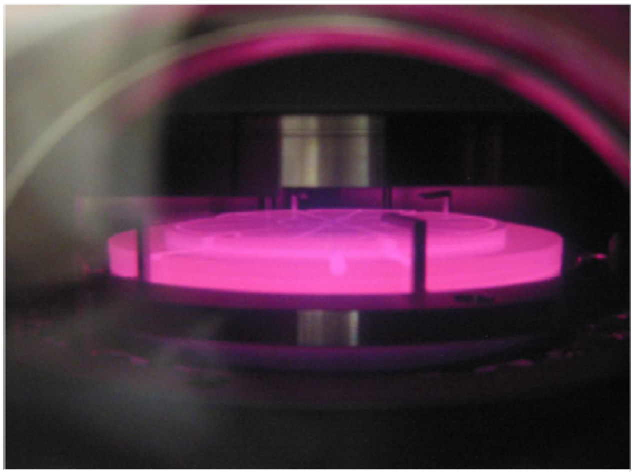

Figure 2.4: Very hot chuck for 150 mm wafer from Oerlikon.

The process also uses a single ceramic target which is sputtered by RF technology directly onto a very hot substrate. To increase the etch rate, the sputter performance is enhanced by a magnetron. This allows for balancing out the requirements for deposition rate, thickness and composition uniformity.

Either one can use one process module for manual single wafer handling or a complete Oerlikon cluster tool CLN200. This sputter equipment is commonly used in wafer processing industry and can be equipped with a maximum number of six modules.

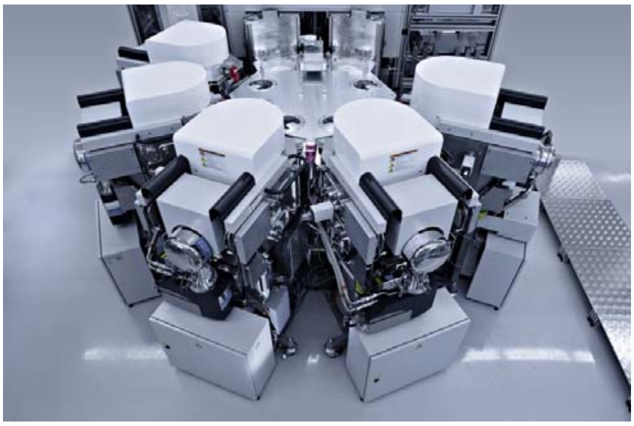

Figure 2.5: Oerlikon cluster tool

2.2.2 Performance

We have shown that it is possible to deposit high quality piezoelectric PZT films ($-e_{31,f}\sim$ between 15 and 20 C/m^2) onto up to 200 mm wafers. The actual throughput at this high film quality is up to 3 wafers/h µm with the potential of > 3.6 wafers/h at further process optimization. The thickness of the films is usually between 1 and 2 µm but if required films with a thickness up several microns can be deposited as well.

2.2.3 Integration

Usually the CLN200 I sputter tool is integrated into a wafer production to allow access to the cassette stations for wafer loading under clean room conditions where the sputter modules are a separated by a clean room wall and located in an area with a slightly higher contamination level (“gray room”).
To operate the system the facility installation has to meet typically the following requirements

System dimensions:	~ 3600 x 5000 x 2000 (W x L x H (mm))
Temperature range:	15 - 35°C
Relative Humidity:	40 – 60 %
Electrical data:	3 x 400/230 VAC 50/60 Hz L1, L2, L3, N and PE
Process gases:	Typically N_2, Ar, O_2, other on demand Purity 5 N or better Operating pressure: 1.4 – 4.0 bar
Compressed air:	5 – 7 bar, 5 µm filtered, dry, oil free
Cooling water:	Conductivity according to Oerlikon water specifications Temperature: 15 – 25°C Inlet pressure at maximum flow 7.5 bar Water consumption depending on configuration, typical range for a tool equipped with 6 module > 200 min-1
Exhaust:	Forepumps have to be connected to facility exhaust system

2.3 Pt sputtering

Pt is also a key process for piezoMEMS and the quality of the bottom electrode is important for the quality of the PZT. A layer stack of Ti / TiO_2 / Pt on top of an oxidized silicon wafer is recommended as the bottom electrode for PZT. The Pt-layer must be highly (111) oriented and the TiO_2 layer must act as an intact diffusion barrier.

2.3.1 Sputter tool for the bottom electrode

Among others both the Oerlikon sputter deposition tool LLS EVO II and the Cluster Tool CLN 200 II can be used. Both tools are industrial deposition tools which offer the required reliability and stability for providing consistent electrode quality. If an electrode post treatment process is not required the CLN200 II will be the preferred tool to produce both the electrode and the piezoelectric layer entirely without any vacuum breakage.

2.4 In-line quality monitoring

Earlier during processing there could only be off-line tests for quality control, partly with dedicated test-wafers and/or test-devices/designs on device wafers. Dedicated test wafers may follow production batches through actual processing steps, but are not able to neither detect design specific problems nor fully map process problems with likely property distributions across wafers and for batch-to-batch control.

2.4.1 In-line quality monitoring system

aixACCT has developed a new high throughput in-line tool for quality control of the piezoelectric thin film (and electrode) properties. The tool, named aixDBLI, combines new and already existing hardware for 150 mm and 200 mm wafers. aixACCT's core technology of optical double beam laser interferometry is combined with a Cascade Microtech auto prober system.

Figure 2.6: In-line quality monitoring system from aixACCT.

The in-line tool enables a much improved process monitoring methodology as it will also allow keeping track of the production yield right after the deposition process. This will reduce production costs of the final MEMS device as the following cost intensive processing steps can be performed on already qualified films. This is also very useful for improving production designs with respect to increased yield through all production steps.

2.4.2 Performance

The fully automated aixDBLI system including a wafer robot allows the measurement of up to 10 wafers per hour using a piezoelectric small or large signal measurement on a 5 point wafer map. The measurement resolution is better than 1 picometer checked by X-cut Quartz measurements with a measurement repeatability better than 1%.

2.4.3 Integration

The aixDBLI system can be used either as a stand alone measurement unit or it can be integrated into a wafer fab production process. This can be established by a standardized interface according to the SEMI standards SECS/GEM. These allow to control the measurement procedure and read out system status and information.

2.5 Design tool integration

Coventor has developed a range of new design and modelling tools to improve the development of piezoMEMS. These MEMS specific software tools enable different levels of modelling, including manufacturing processes, device and system design. Interfaces to other standard design tools are available. Details on Coventor’s design tools for piezoMEMS are described in Chapter 3.1 below.

2.6 CMOS materials compatibility

PZT, Pt- and Au are materials that are not CMOS compatible. In many fabs the use of such materials must be strictly controlled to allow for simultaneous processing of components that need a CMOS compatible lab. For example, minute quantities of Pt or Au may contaminate both tools and clean wafer batches beyond repair.

Limitations on accepted materials vary between different labs and foundries and have to be addressed when planning the fabrication.

3 DESIGN

3.1 Design tools

Different tools for the design and modelling of piezoMEMS have been developed and are available. These software tools are calibrated to the PZT processes and enable engineers to simulate and optimize piezoMEMS designs before committing to build-and-test cycles. Coventor's MEMS+ and CoventorWare provide a design and simulation platform for MEMS designers, enabling them to simulate end-product performance specs such as sensitivity, linearity, frequency response, signal-to-noise, and temperature stability. SEMulator3D is a unique modelling tool for virtual fabrication, enabling them to review designs and detect process issues in advance of actual fabrication.

For mask layout any design tool which can generate a GDSII-file is appropriate, e.g. L-Edit. For L-Edit, also a piezoMEMS mask layer setup is available.

3.1.1 Design exploration and system-level simulation

The design platform MEMS+ allows to, quickly explore design alternatives, and to optimize performance with high accuracy. With Coventor's design flow the PZT technology comprising material and process data is already defined. To start with, a model of the piezoelectric device is constructed in MEMS+. Here, the MEMS designer works in a 3D graphical environment to assemble a parametric model using high-order MEMS-specific finite elements (piezo-mechanical shells). Each element is linked to the process description and material database so that piezoelectric material properties and electrodes are assigned automatically. The high-order elements give a precise mathematical description of the device physics using a low number of degrees of freedom. This enables rapid, accurate simulation of the device physics in Matlab/Simulink, and the ability to easily co-simulate the device with the conditioning circuit in Cadence Virtuoso. For example, the designer can tune the piezoMEMS device dimensions to attain a maximum actuation displacement or a certain resonance frequency before simulating the device with different electronic circuits to compare the performance of each type.

3.1.2 Design refinement and validation

Further detailed modelling can be undertaken using CoventorWare's field (or Finite-Element)) solvers to investigate details of the design. For example, the design can be checked for high stress areas that may lead to breakage when the device is overloaded due to a shock. Gas damping coefficients can also be simulated and included in the MEMS+ model to accurately predict the Q-factor. An additional benefit is that simulation results from MEMS+ and CoventorWare can be verified against each other. Simulating piezoelectric harmonic analysis with a linear resistive load is one such example of a point of comparison between both tools. Coventor's solution for piezoelectric devices combines MEMS+ and CoventorWare to provide hybrid solution that solves the coupled and multi-domain physics not addressed with traditional point tools.

3.1.3 Virtual fabrication

The 3D process modelling tool SEMulator3D enables virtual fabrication of piezoMEMS processes. Based on voxel (volumetric pixels) modelling technology, SEMulator3D has the ability to emulate complete process flows and build highly detailed, virtual prototypes. Input to the tool is only the 2D masks in GDSII format. Description of the calibrated PZT fabrication process is already available.

SEMulator3D offers a productive methodology that enables engineers to understand and communicate process flow and device design through interactive visualization and quantitative measurements. Areas of usage include process documentation, process modelling and optimization, process communications with foundry customers and piezoMEMS design verification prior to actual fabrication.

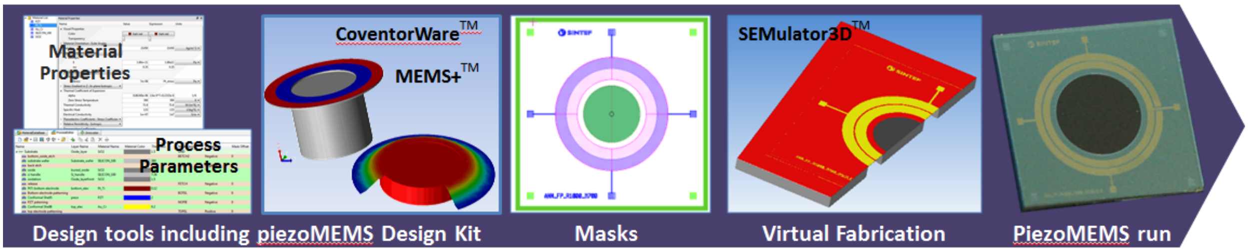

Figure 3.1: PiezoMEMS design flow integrating Coventor tools suite

All Coventor tools have process entry user interfaces that allow import of ready-to-use and calibrated piezoMEMS PZT technology template files, e.g. MoveMEMS SINTEF process.

3.2 Material specifications

3.2.1 Wafer specifications

The process starts with a (bonded) silicon on insulator (SOI) wafers with an 8 µm device layer. The device layer of the SOI wafer defines together with the deposited layers the thickness of the resonating structures. 8 µm is found to be a good compromise between stiffness of resonators and mechanical strength during manufacturing. However, other thicknesses are available on demand.

Table 3.1: Example of wafer specification used for piezoMEMS

Device layer	**Diameter**	150 mm
	Type/Dopant	N/Phos
	Orientation	<100>
	Thickness	8 um
	Resistivity	1-10 Ohmcm
	Finish	Polished
Buried thermal oxide	**Thickness**	500nm
Handle wafer	**Type/Dopant**	N/Phos
	Orientation	<100>
	Resistivity	1-10 Ohmcm
	Thickness	500 µm
	Finish	Polished

3.2.2 CSD PZT film specifications

The electromechanical properties of a film are different from those in bulk materials as the film is clamped to the substrate. The processing steps and in particular the thin film deposition process will also introduce a specific material quality. Deconvolution of real material coefficients often requires detailed knowledge of the elastic constants of the materials involved in the system, constants that may or may not be known. Hence, when dealing with thin film structures it is more convenient to operate with "effective" coefficients:

$$e_{31,f} = \frac{d_{31}}{s_{11}^E + s_{12}^E} = e_{31} - \frac{c_{13}^E}{c_{33}^E} e_{33}$$

$$d_{33,f} = d_{33} - \frac{2 s_{13}^E}{s_{11}^E + s_{12}^E} d_{31}$$

With d_{xx} being the piezoelectric coefficient, e_{xx} the piezoelectric modulus, s_{xx} the elastic coefficient, c_{xx} the elastic constant in the direction given by the indices.

Films and devices are characterized electrically by measuring the electrical permittivity, CV, ferroelectric hysteresis and piezoelectrically by measuring the transversal piezoelectric charge coefficient $e_{31,f}$ with a 4-point bending measurement setup. Material parameters may vary according to the deposition method and level of defects.

Table 3.2: Parameters for the PZT film

Parameter	Value
E, Young's modulus	73 GPa
Poisson's ratio	0.288
Linear CTE	2.5 ppm
Density	7750 kg/m^3
Stress for non-poled PZT	130-160 MPa
Stress for poled PZT	150-200 MPa
Relative permittivity, , ε_r	1300±100
Dielectric dissipation factor, tanδ	0.029
Breakdown field (typical)	> 300 kV/cm
-$e_{31,f}$ @ 1 Hz, zero bias	14-15 C/m2
$d_{33,f}$	110-125 pm/V

3.2.3 Breakdown field

There is no standard test for breakdown field. We use two different breakdown field test procedures. First, as shown in Figure 3.2, we apply a unipolar triangular waveform with increasing amplitude and intermittent measurement of $e_{31,f}$ coefficient.

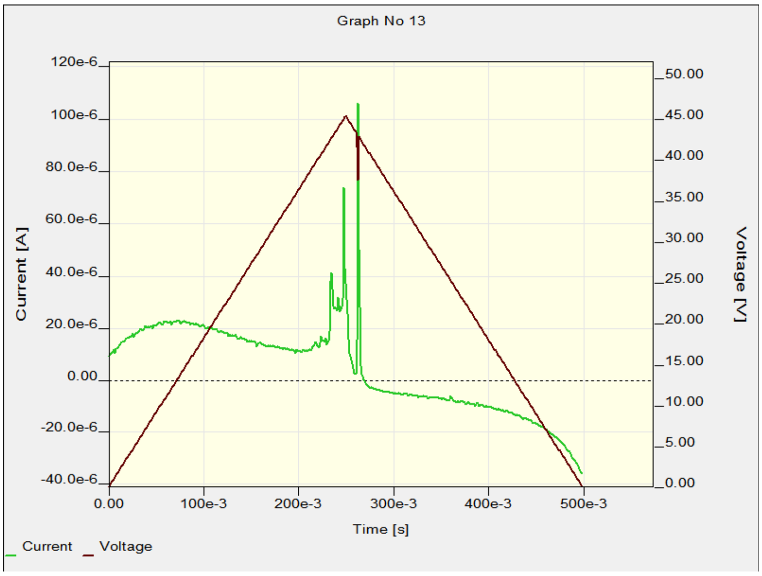

Figure 3.2: Example of breakdown field. At 45V a local dielectric breakdown occurs. After this breakdown test it was still possible to measure an $e_{31,f}$ coefficient.

The second breakdown test is destructive, as shown in Figure 3.3. A voltage ramp of 1V/second is applied to the sample until a complete dielectric breakdown occurs.

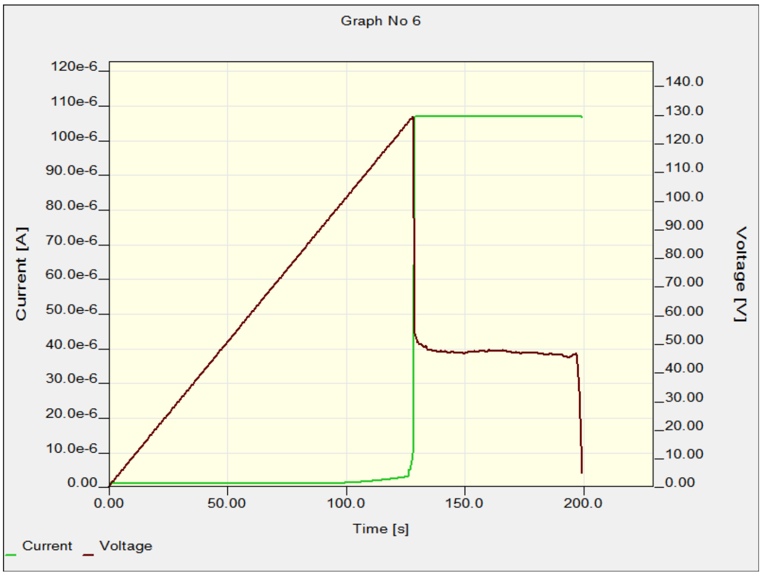

Figure 3.3: Breakdown test using voltage ramp of 1V/second. A 4µm thick CSD PZT film shows dielectric breakdown at 130V (325 kV/cm 65 V/2 µm).

The typical breakdown field is in excess of 325 kV/cm (65 V/2 µm), measured on test structures with standard electrode size.

3.2.4 Poling

For many applications, the ferroelectric PZT thin film material needs to be polarized. The material is generally poled at 150 kV/cm for 5-10 min at 100°C. Normally the bottom electrode is chosen to be negative.

3.2.5 Mechanical parameters for other layers than PZT

Mechanical parameters for the different layers are given in the table below. A full set of parameters is available as a part of the Process Development Kit from Coventor.

Table 3.3: Mechanical material parameters

Material	Young's modulus (GPa)	Built-in stress (MPa)	Mass density (kg/m^3)
Si	160	-	2331
SiO_2 (thermal oxide)	70	-300	2200
Pt	168	700	21450
Au	78	300	19300

3.3 Mask layer overview

The piezoVolume designs are of three basic types, based on end user specifications, design rules and processing limitations. The three processing routes available are:

A. Sensor-type with inter digital electrodes, without bottom electrode
B. Sensor-actuator types with bottom electrode
C. As B, including polymer isolating layer and two-layer top metal for routing

For more details about the processing routes, see chapter 4.1.

Some masks can be shared between the processing routes to reduce the mask cost during prototyping. As specified in Table 3.4 only some steps need an additional mask.

Table 3.4 Mask layer definition

Mask layer name	Description	Process type	Dark/Clear field
TOPEL_FINGER	This mask will contain the patterns for the top electrode	A	Clear Field
PASOPEN	This mask will contain the patterns for openings in passivating layer down to TOPEL	A	Dark field
METPAD	This mask will contain the patterns for pads down to TOPEL, might be lift-off	A	Clear field or Dark field
TOPEL	This mask will contain the patterns for the top electrode	B,C	Clear Field
NOPIE	This mask will contain the patterns for the PZT structures	B,C	Dark field
BOTEL-NOPT	This mask will contain the patterns for the bottom electrode	(B), C	Dark field
DIELOPEN	This mask will contain the patterns for opening of via-contacts to TOPEL and BOTEL through the isolating layer	C	Dark field
METAL3	This mask will contain the patterns for the bond pads and electrical contacts to TOPEL and BOTEL.	C	Clear Field
BACKOXIDE	This mask will contain the patterns to remove SiO2 on the backside where the membranes will be	A,B,C	Dark field
BETCH	This mask will have square, circular or rectangular openings for the definition of the etching of membranes from the backside. This etch will stop on the BOX layer in the SOI wafers	A,B,C	Dark field
FETCH	This mask will have patterns for possible release etch of cantilevers etched from the front side (only necessary for release etch)	B,C	Dark field

3.4 Layout Rules

General layout rules:

- No pattern should be closer than 10 mm from the edge
- Standard bond pad size is 200 × 200 µm^2

Table 3.5: Design rules for each mask layer

Mask layer name	Design rule
TOPEL and TOPEL_FINGER	Inter digital electrodes: minimum line width and spacing of 8 µm
	Conductor lines: minimum line width of 10 µm, 20-40 µm is preferred
	For process B bond pads should be considerably smaller than active area, but not smaller than 120x120 µm^2
NOPIE	Minimum overlap to TOPEL is 5 µm, 10 µm is preferred
	Minimum distance between openings is 20 µm
	TOPEL has to be removed everywhere where NOPIE is to be etched
BOTEL-NOPT	Minimum overlap to NOPIE 10 µm, 20 µm is preferred
	NOPIE has to be open everywhere where BOTEL-NOPT is open
PASOPEN	Minimum 50 µm to inter digital electrodes
METPAD	-
DIELOPEN	Openings only on top and bottom electrode (TOPEL and NOT BOTEL_NOPT). Minimum 6 µm to metal edge, 10 µm is preferred
	Minimum contact opening 60x60 µm^2
METAL3	Minimum overlap DIELOPEN 6 µm, 10 µm is preferred
	Metal pad should be larger than the opening in the DIELOPEN
	Conductor lines: minimum line width of 15 µm, 20-40 µm is preferred
BACKOXIDE	20 µm larger openings than BETCH
BETCH	Se chapter 3.4.1
	BACKOXIDE has to be open everywhere where BETCH is open
FETCH	-

3.4.1 Design rules for DRIE

Exposed Si should not exceed 20% of the wafer area, as this will reduce the etch rate considerably.

The minimum dimension of the smallest DRIE structure is in general 20 µm. The membrane size should preferably not be smaller than 50 µm. The largest dimension of the largest DRIE structure may be up to 5 mm.

Very large and very small DRIE structures together on the same wafer are a challenge. If the difference in dimensions is large, the etch profiles and etch depths will be significantly different even if the structures are placed far apart. Preferably each design should be revised by a RIE expert.

3.5 Design for manufacture

Design for Manufacturing (DFM) is an approach that considers manufacturability during the design process. Broadly, DFM includes organizational changes, systematic design principles and a common CAD methodology and framework for evaluating product designs (Ref 1).

The Coventor tool suite offers a platform dedicated to MEMS design starting from technology and manufacturing information. This design flow specificity enables a better integration of DFM principles into MEMS fabrication.

The Coventor Design kits include the material properties, process descriptions, layout templates and Design Rules Check (automatic or manual). Those are references and tools for the designer to create a device in a platform which includes manufacturing rules and limitations. Recent versions of piezoMEMS PZT design kits are available for all tools described in 3.1. In MEMS+ design kit, statistical data on fabrication steps (thickness or over-etch values for examples) given by the foundry can be added and used in simulations to run yield analysis or study performances of a random set of devices (e.g. Monte Carlo algorithm).

Virtual manufacturing with SEMulator3D allows checking masks prior to fabrication. Using the technology description, any layout can be built in 3D and the viewer enables direct and easy validation of each GDSII mask to be used in the clean room.
The last point relevant to DFM is covered by FEA tool CoventorWare. It concerns stress and reliability analyses. Knowing material characteristics the designer can run simulations for specific thermal or mechanical behaviour under boundary conditions applied during the fabrication process like accelerations, maximum temperature or pressure. These conditions may be specific to the foundry and a certain type of analyses can be then recommended. Some of these analyses may also be run in MEMS+ if statistical data (huge amount of calculation points requested) are used.

4 FABRICATION

4.1 Introduction

This chapter gives an overview of the process, showing how the piezoVolume devices are manufactured according to a documented process chain.

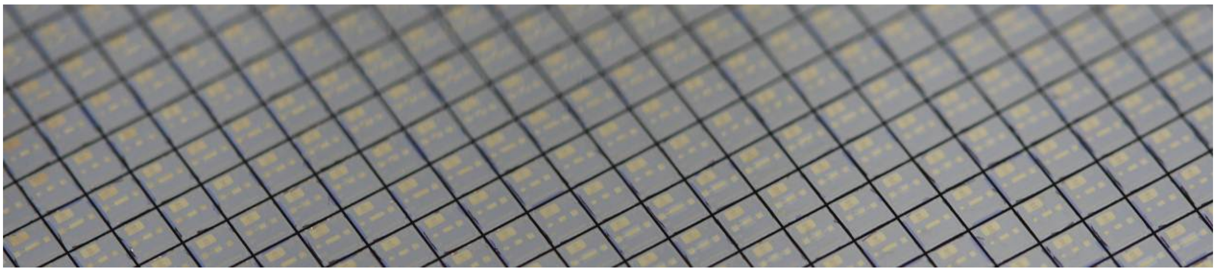

Figure 4.1: piezoVolume devices (also termed chips or dies) after the wafer has been diced.

A silicon-on-insulator (SOI) wafer is the starting point, where the buried oxide is employed as an etch stop for the back side bulk etch. Thermally grown SiO_2 serves as a barrier towards the Si, but also as a stress compensation layer as the compressive stress in the SiO_2 can be utilized to cancel the tensile stress in the later deposited layers (mainly from PZT).

The main processing routes are defined by the use of bottom electrode and top electrode or only top electrodes.

As mentioned in Chapter 3.3, the three processing routes available are:

A. Sensor-type with inter digital electrodes and a barrier layer instead of bottom electrode
B. Sensor-actuator types with bottom electrode
C. As B, including patterned bottom electrode and a polymer isolating layer and two-layer top metal for routing

4.2 Process overview for type A –without bottom electrode

1. Thermal oxidation
2. Deposition of piezoelectric stack
    a. Barrier layer deposition
    b. PZT deposition
    c. Top electrode deposition
3. Back side patterning of SiO_2,
   MASK: BACKOXIDE
4. Patterning of top electrode
   MASK: TOPEL_FINGER
5. Deposition and patterning of passivation layer
   MASK: PASOPEN
6. Deposition and pattering of metal pads
   MASK: METPAD

7. Back side etch
   MASK: BETCH. It is in principle possible to use both DRIE and TMAH in this step but the device density is much improved by DRIE where you can avoid the angled sidewalls.
8. Dicing

4.3 Process overview for type B and C –with bottom electrode (B and C) and two-layer top metal (C)

1. Thermal oxidation
2. Deposition of piezoelectric stack
   a. Bottom electrode deposition
   b. PZT deposition
   c. Top electrode deposition
3. Back side patterning of SiO_2
   MASK: BACKOXIDE
4. Patterning of top electrode
   MASK: TOPEL
5. Patterning of PZT
   MASK: NOPIE

Now type B is finished except for back side etch.

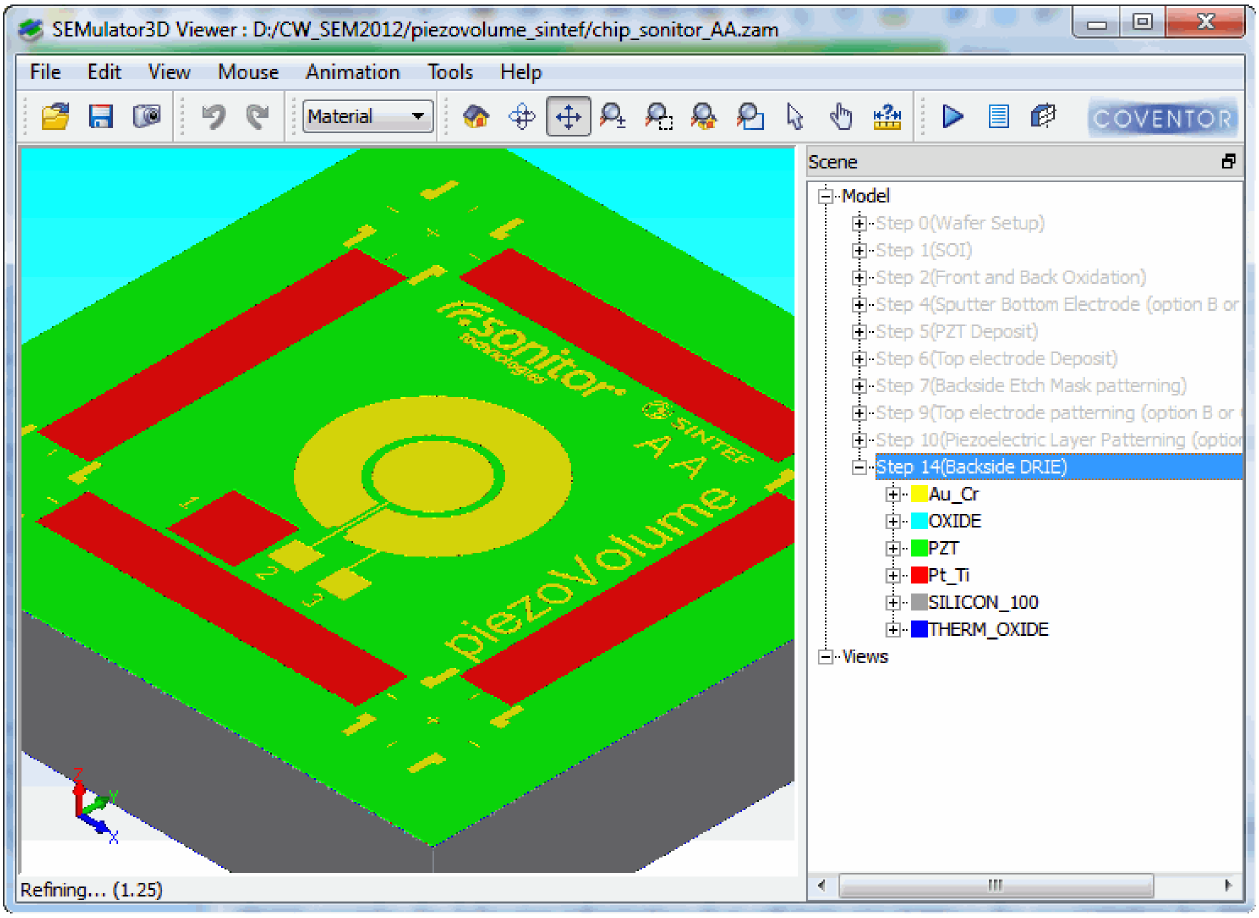

Figure 4.2: Device, process type B

6. (only C) Patterning of bottom electrode
   MASK: BOTEL-NOPT
7. (only C) Deposition and patterning of isolating layer
   MASK: DIELOPEN
8. (only C) Deposition and pattering of top metal
   MASK: METAL3
9. Back side etch,
   MASK: BETCH. It is in principle possible to use both DRIE and TMAH in this step but the device density is much improved by DRIE where you can avoid the angled sidewalls.
10. Dicing

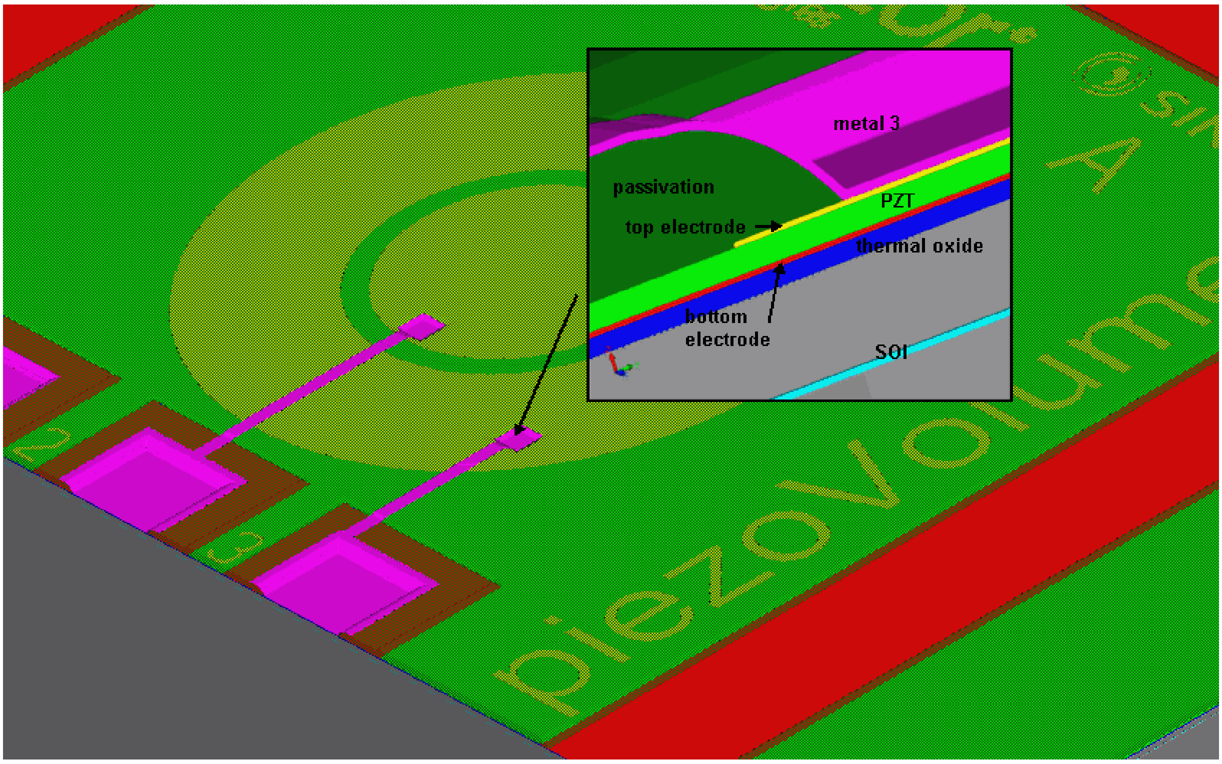

Figure 4.3: Device, process type C where passivation layer is set transparent (not in the zoomed cross section).

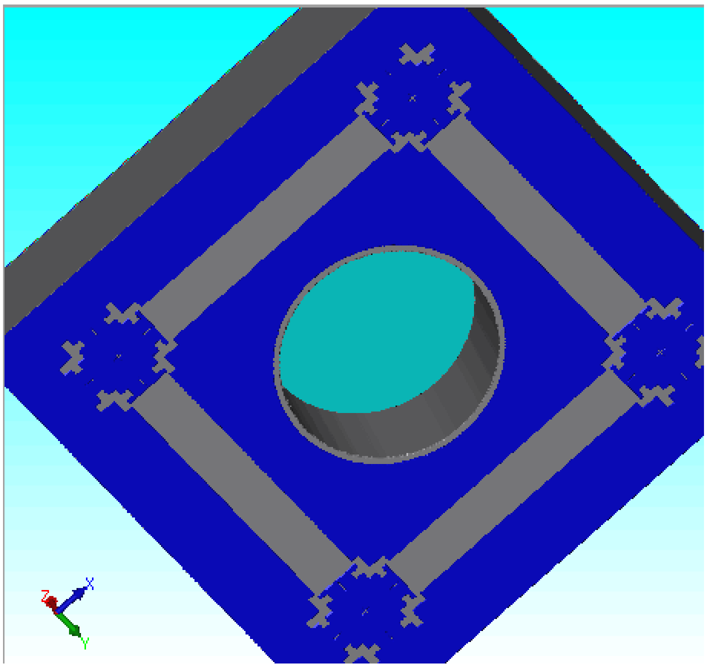

Figure 4.4: Backside of device with the backoxide etch (dark blue) and Silicon DRIE stopped at buried oxide (light blue)

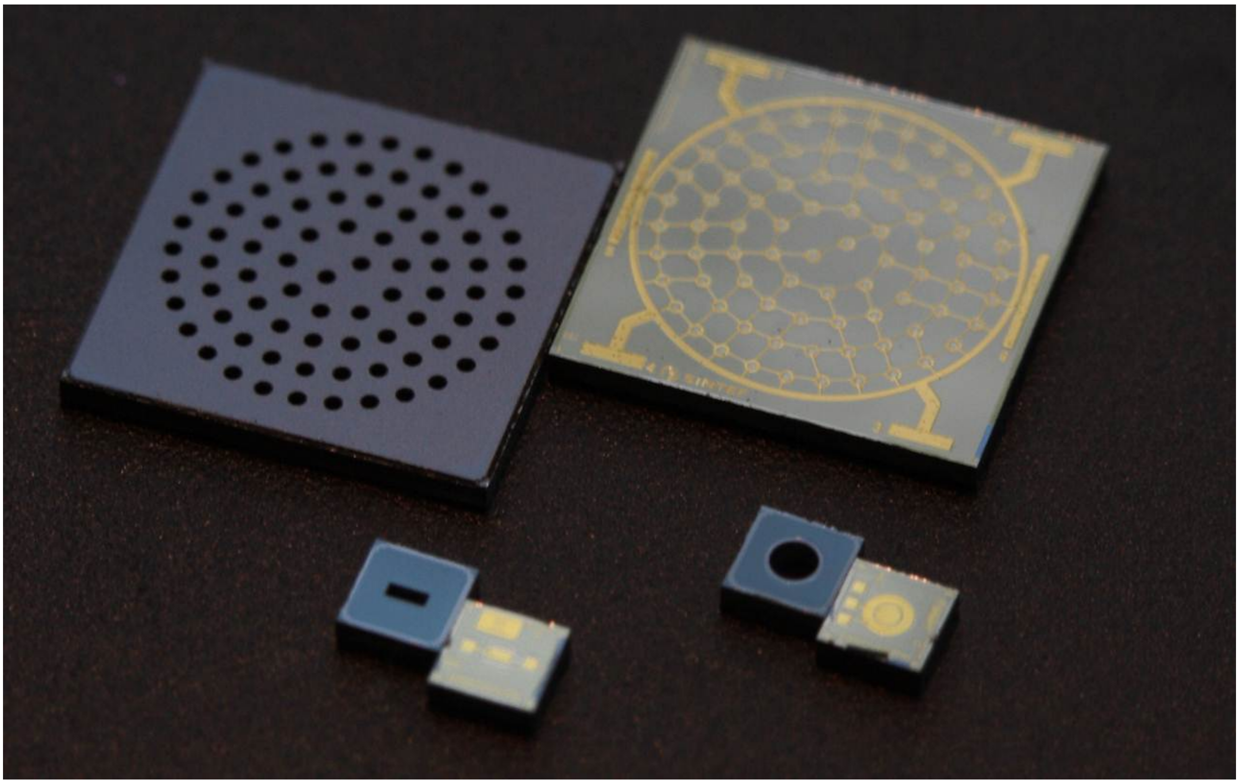

Figure 4.5: piezoVolume devices ready for packaging.

4.4 Fabrication strategy for CMOS compatibility

There can be several strategies to overcome this issue. One is to define parts of the cleanroom where additional materials are allowed and the wafers can be processed. All process steps that acquire CMOS-compatible equipment, such as thermal oxidation, must then be performed prior to Pt and PZT deposition.

4.5 Integration of piezoMEMS with higher level system and possible passivation

4.5.1 Wire bonding

One should preferable use thick (minimum 500 nm) Au-pads for wire bonding. It is preferred to have metal bond pads on bare silicon oxide and not on top of PZT.

4.5.2 Packaging for demanding environments

Direct exposure of the wafer's top side to various (conducting or chemically aggressive) fluids and gases requires additional process layers. Polyimide and Au may be used as additional barriers and packaging materials. One solution is to use additional layers of isolating/Au layers on top of the PZT stack.

As an example, processed 150 mm wafers could be bonded with a patterned glass wafer prior to dicing, for enhanced protection by encapsulating the fragile devices, see Figure 4.6. Advanced glass pattering can include TGV (through glass vias) and/or vias in Si as needed for e.g. acoustic coupling with the environment.

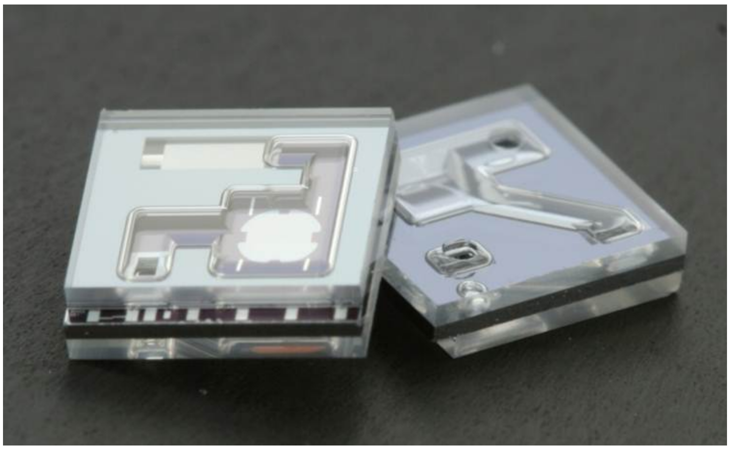

Figure 4.6: Flow sensor from MicroBuilder. A processed Si wafer has been bonded to two patterned glass wafers.

The backside of the processed wafers may be exposed to various exposures, e.g. water, under moderate pressures without further protection. The burst pressure of the membranes must be calculated. For other applications also the backside of the device can be protected by a bonded glass wafer- or by bonding directly to a ceramic or silicon substrate.

5 REFERENCES

1. Designing Manufacturable MEMS in CMOS Compatible Processes - Methodology and Case Studies, G. Schröpfer, M. McNie, M. da Silva, R. Davies, A. Rickard, F-X. Musalem, MEMS, MOEMS, and Micromachining, Strasbourg, France, 26-30 April 2004