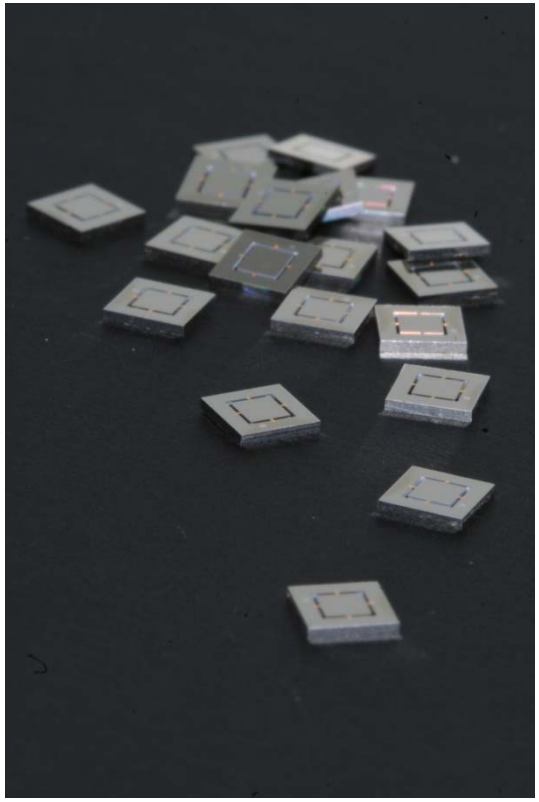
piezoVolume

High volume piezoelectric thin film production process for microsystems

Frode Tyholdt
SINTEF

Background

- Small and medium companies/ Universities have ideas where PZT thin film technology is needed
  - But, often no means to develop/produce piezoMEMS
- Companies are looking for high volume solutions
  - Prototyping
  - Deposition
  - Fabrication
- Reliable deposition/fabrication solutions will increase the interest in piezoMEMS technology even more

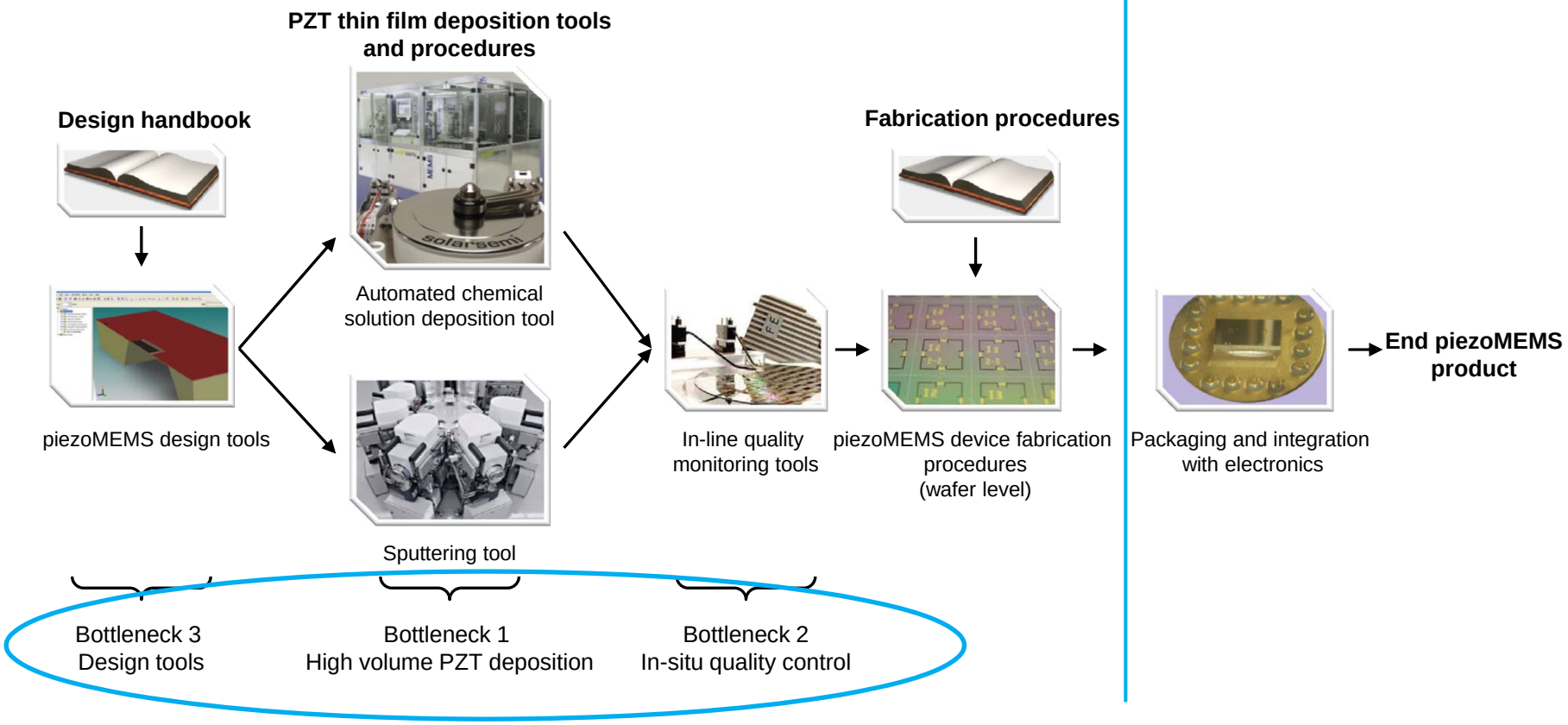


piezoMEMS accelerometers

FP7 piezoVolume (2010 – 2012)

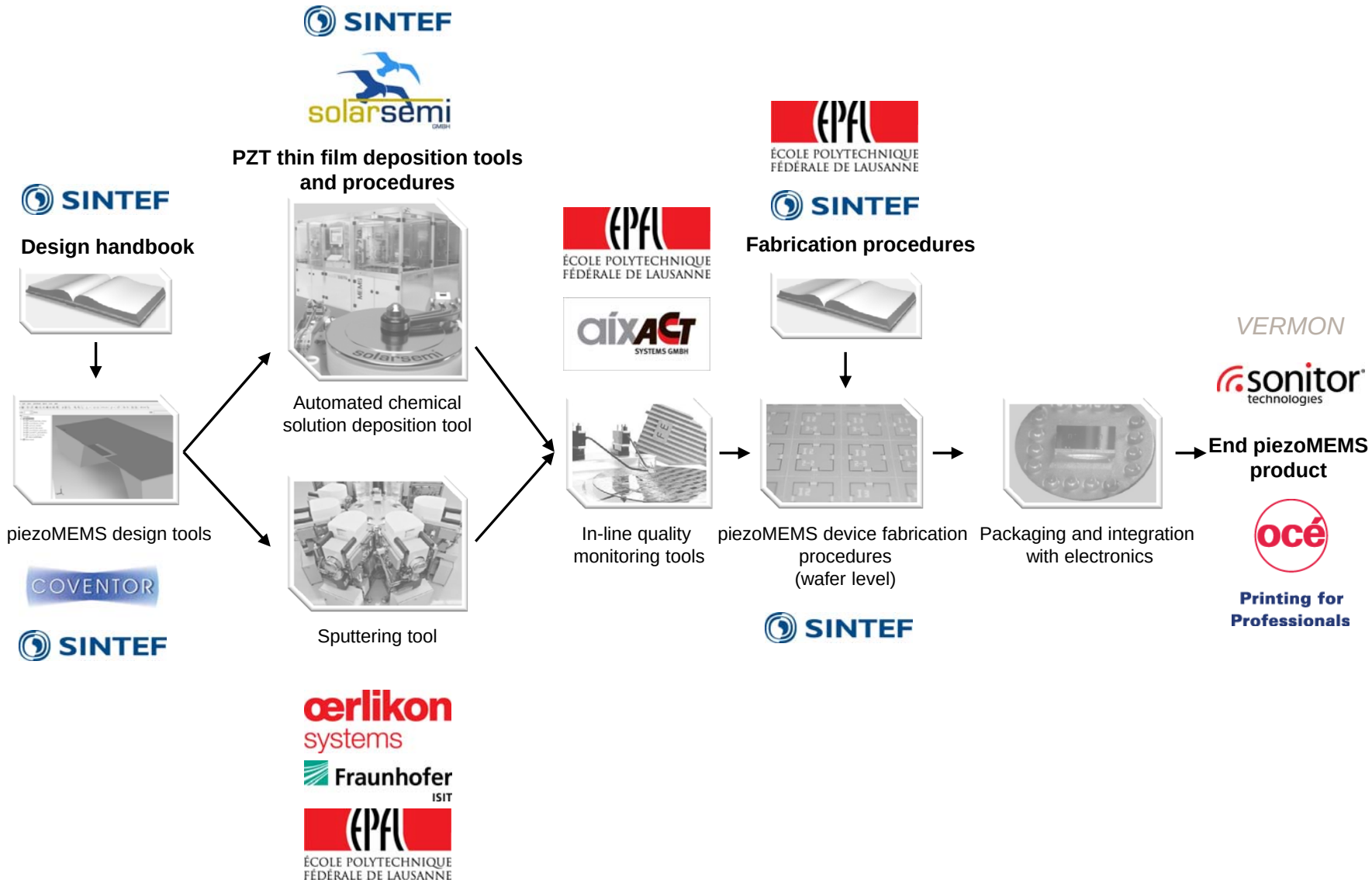
High volume piezoelectric thin film production process for microsystems

5,14 M€ project

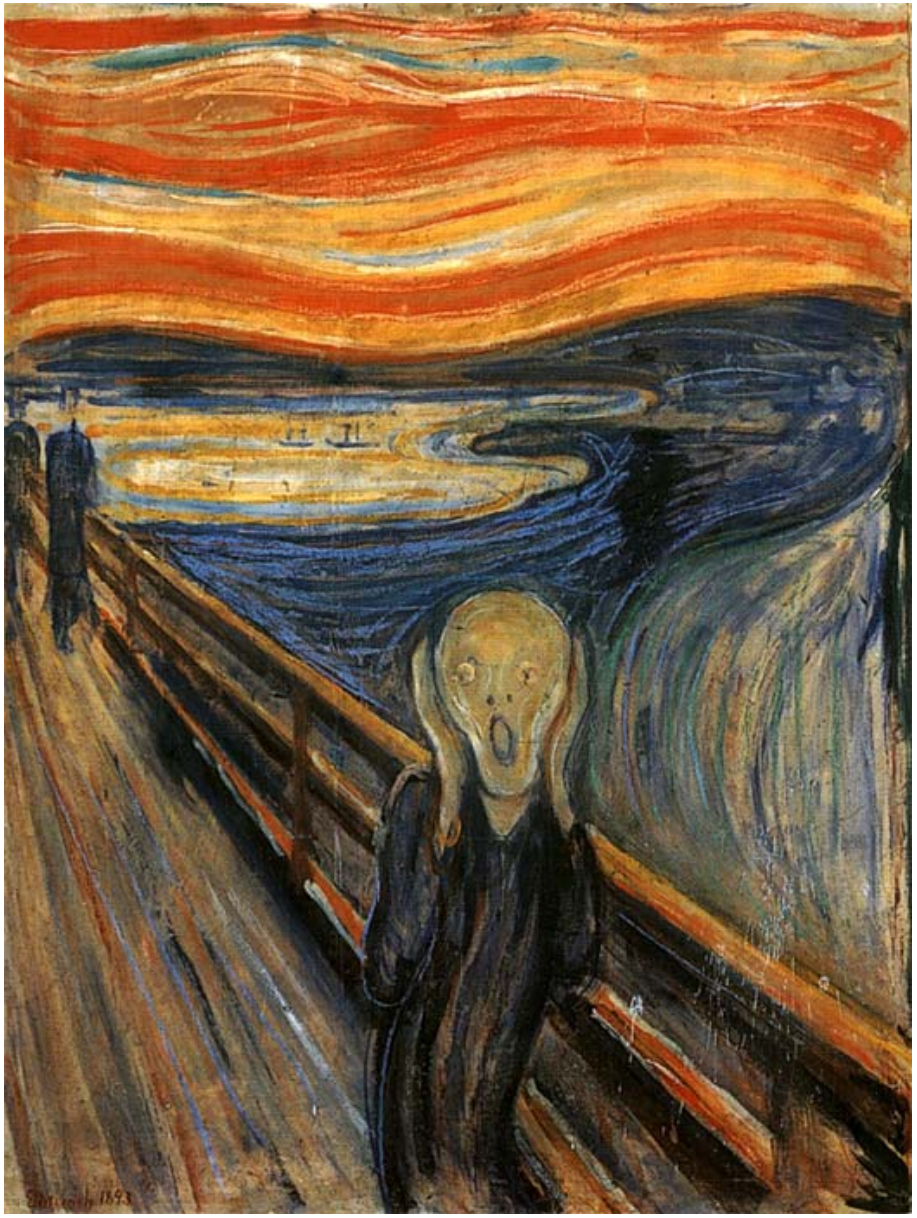


Project focus ends here

piezoVolume – partners



"Dear cleanroom mananger. I want to process PZT in your lab"

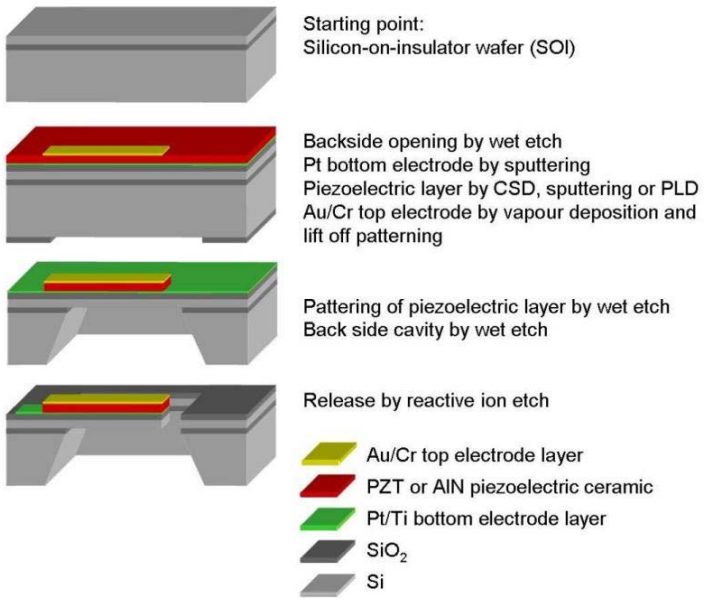


Scream - Edvard Munch 1893

piezoMEMS design and fabrication rules

- Tool integration in lab
  - CMOS compatibility can be obtained
- Material specifications and design guidelines
  - Material parameters
  - Design guidelines and process limitations
  - Basic definition of lithographic masks
- Most of it public

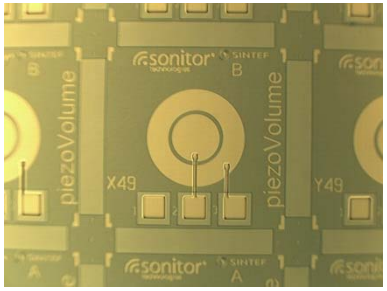
The piezoVolume base processes



3 electrode configurations

Standard

Interdigital



Cross-routing enabled

piezoMEMS specific design and modelling tools

- Lower entrance barrier and become productive more quickly, focusing on your MEMS design instead of your software
- Develop MEMS devices at a lower cost
- Efficiently design new MEMS products, moving them quickly from development into production
- Rapidly explore and optimize design and process options
- Adapt existing designs and processes to new markets
- Efficiently accommodate customer-requested design changes
- Save fab cycles during development and improve yield

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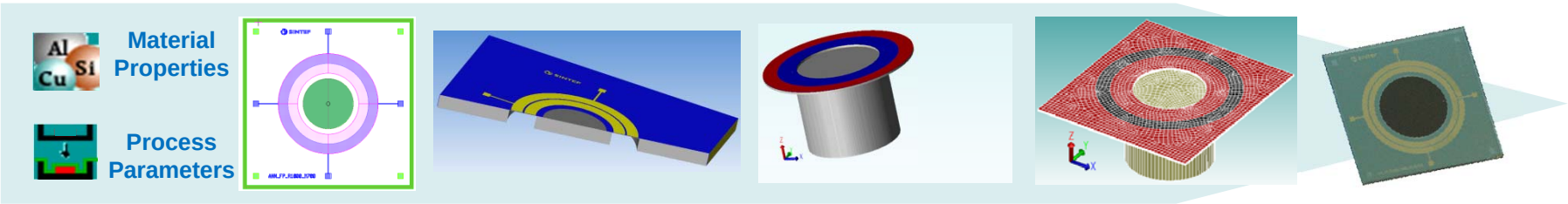
MEMS+ | CoventorWare | SEMulator3D



Process details | DESIGNER™ | SEMULATOR3D TM | MEMS+ TM | ANALYZERTM | PiezoMEMS run

piezoMEMS specific design and modelling tools

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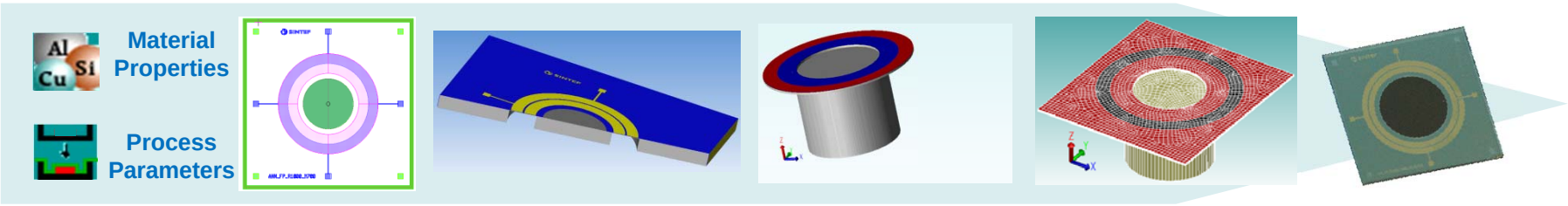
- **Key Features**
  - 3D parametric library of standard (piezo)MEMS components
  - Integration with traditional ICs and MEMS
  - Integration with FEM software
  - Material parameters included in process design kit (PDK)

See poster P10



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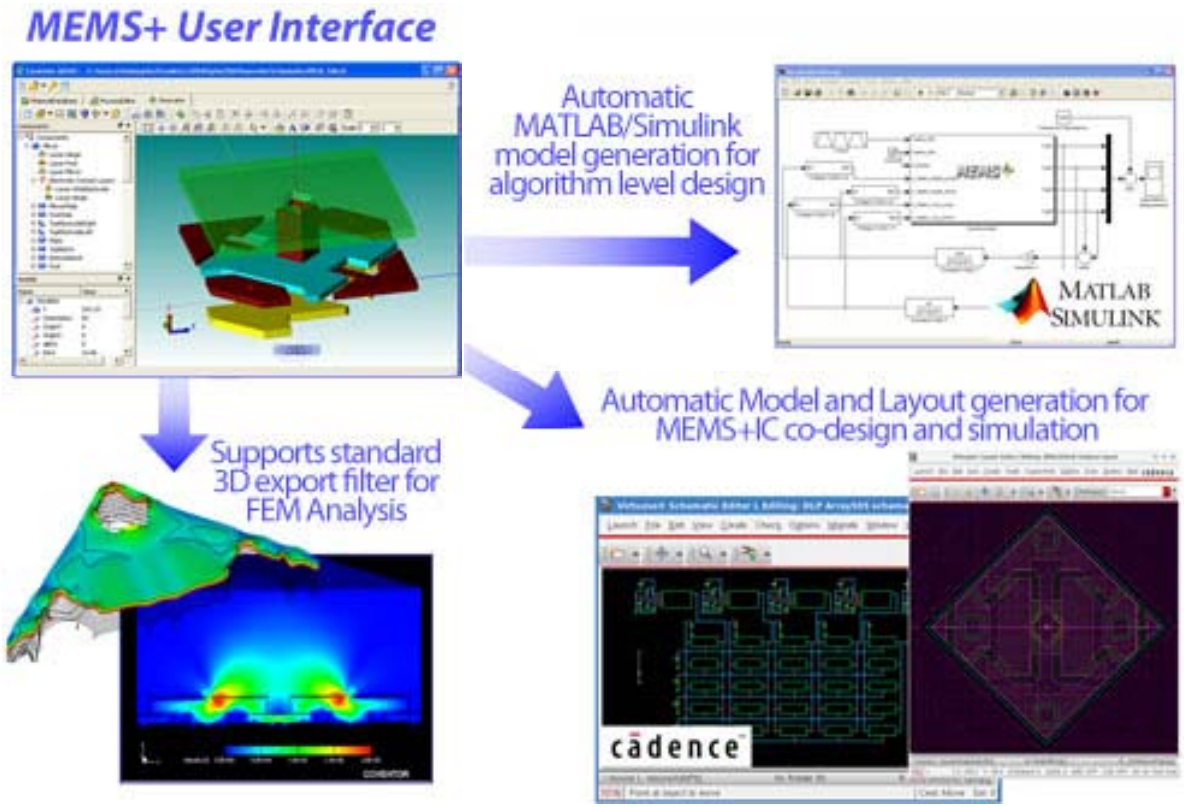
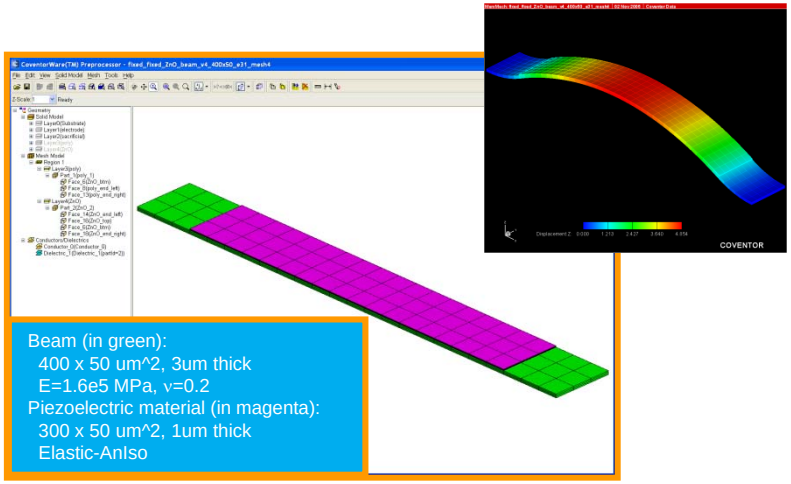
piezoMEMS design platform – MEMS+

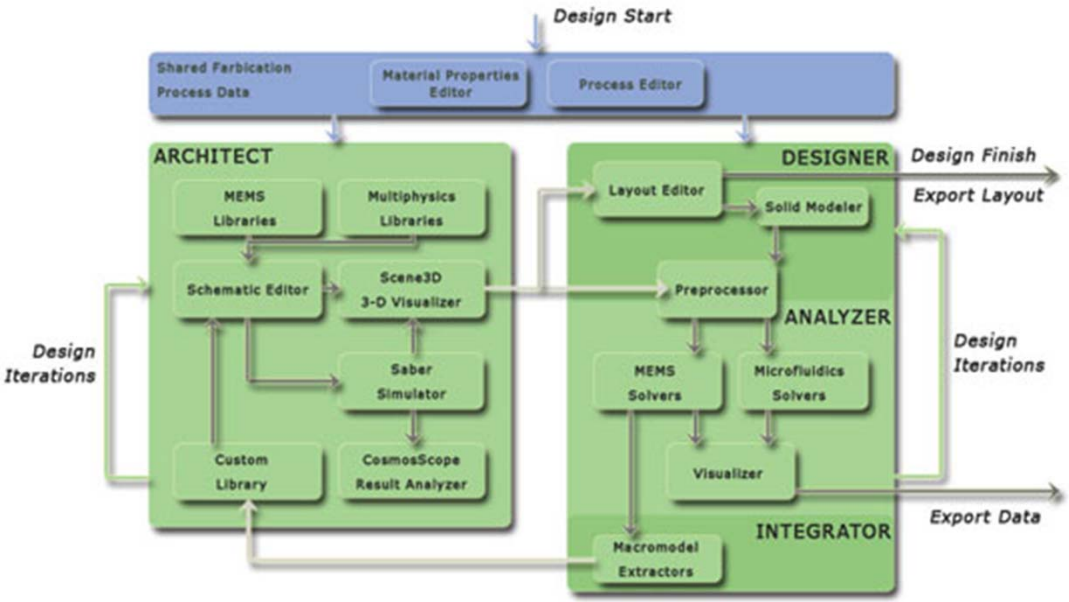


CoventorWare

- Complete software with 4 main packages
  - Architect3D
    - behavioural modelling
  - Designer
    - process specific design
    - Export of litho masks
  - Analyzer
    - FEM modelling
    - Visuliazation
  - Integrator
    - Extraction of linear/non-linear behavioural models



piezoMEMS beam in Coventorware ARCHITECT.



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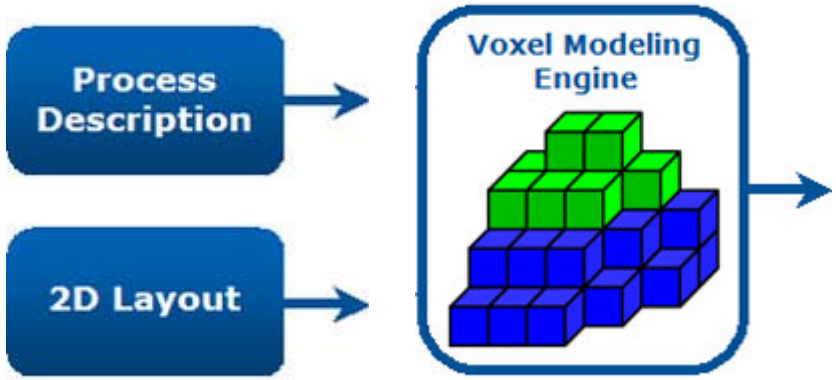
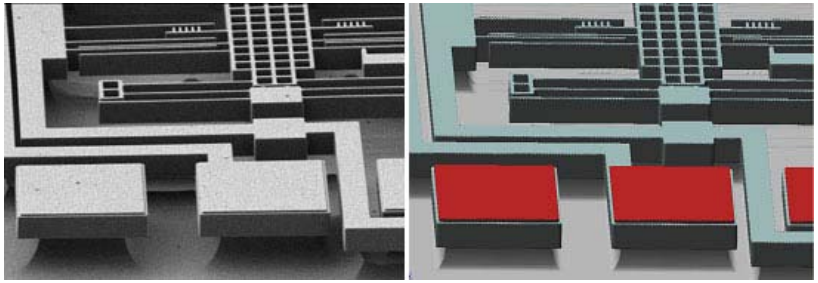
Virtual manufacturing of piezoMEMS – SEMulator3D





Virtual manufacturing of MEMS bond pads and comb drive.
Courtesy X-FAB Semiconductor Foundries, AG.

- 2D masks + description of fabrication process to create a voxel based 3D solid model.

- **Save Money** by finding problems before fabrication.
- **Enhance communication** with highly detailed, interactive 3D models.
- **Reduce time-to-market** and gain a competitive advantage.
- **Improve documentation** and reduce document creation effort.
- **Enhance Yield** through improved design rules and defect modelling.

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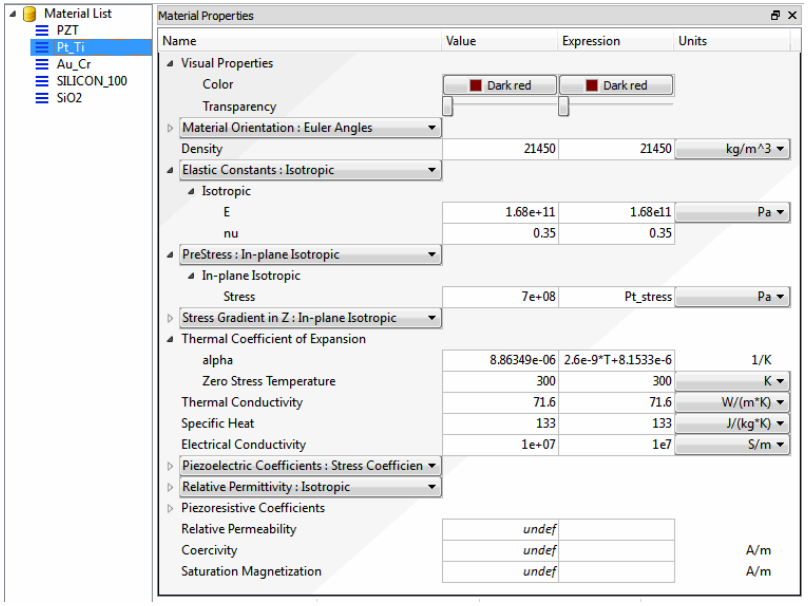
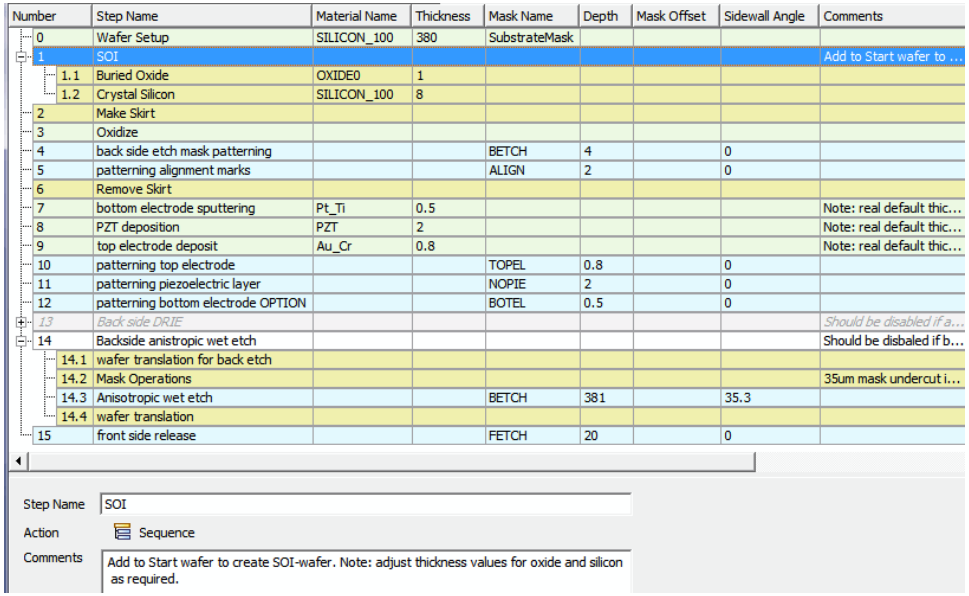
piezoMEMS process design kit (pdk)

- Design Kits for SINTEF MoveMEMS PZT-based process including:
  - Material Databases storing relevant physical properties of materials meaningful for simulation and/or virtual fabrication
  - Process files describing the major fabrication steps stack
  - Implemented and documented in the latest releases of COV tools.





Number	Step Name	Material Name	Thickness	Mask Name	Depth	Mask Offset	Sidewall Angle	Comments
0	Wafer Setup	SILICON_100	380	SubstrateMask				
1	SOI							Add to Start wafer to ...
1.1	Buried Oxide	OXIDE0	1					
1.2	Crystal Silicon	SILICON_100	8					
2	Make Skirt							
3	Oxidize							
4	back side etch mask patterning			BETCH	4		0	
5	patterning alignment marks			ALIGN	2		0	
6	Remove Skirt							
7	bottom electrode sputtering	Pt_Ti	0.5					Note: real default thic...
8	PZT deposition	PZT	2					Note: real default thic...
9	top electrode deposit	Au_Cr	0.8					Note: real default thic...
10	patterning top electrode			TOPEL	0.8		0	
11	patterning piezoelectric layer			NOPIE	2		0	
12	patterning bottom electrode OPTION			BOTEL	0.5		0	
13	Back side DRIE							Should be disabled if a...
14	Backside anistropic wet etch							Should be disbaled if b...
14.1	wafer translation for back etch							
14.2	Mask Operations							35um mask undercut i...
14.3	Anisotropic wet etch			BETCH	381		35.3	
14.4	wafer translation							
15	front side release			FETCH	20		0	

Step Name: SOI

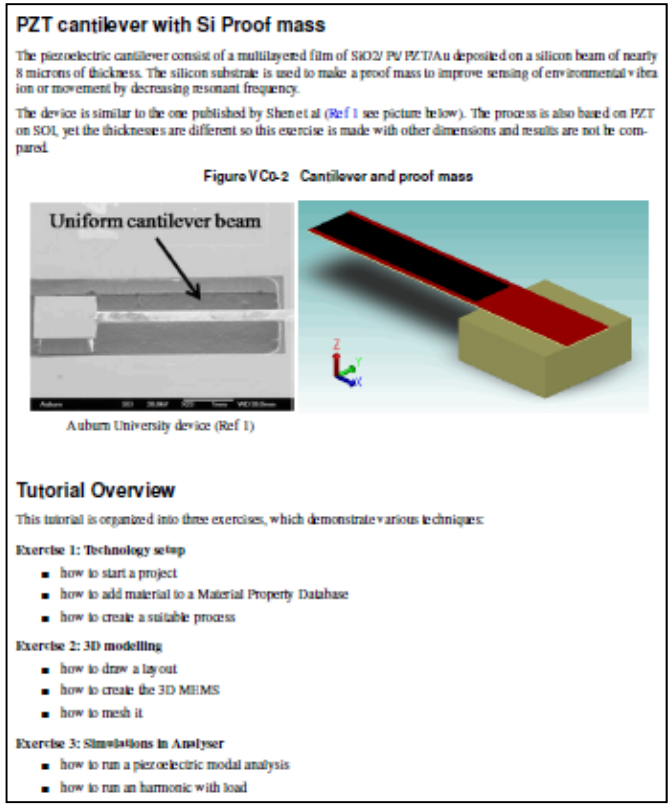
Action: Sequence

Comments: Add to Start wafer to create SOI-wafer. Note: adjust thickness values for oxide and silicon as required.

Software tutorials

Energy Harvester design in **CoventorWare**

Step by step manual



PZT cantilever with Si Proof mass

The piezoelectric cantilever consist of a multilayered film of SiO2/ Pt/ PZT/Au deposited on a silicon beam of nearly 8 microns of thickness. The silicon substrate is used to make a proof mass to improve sensing of environmental vibration or movement by decreasing resonant frequency.

The device is similar to the one published by Shen et al (Ref 1 see picture below). The process is also based on PZT on SOI, yet the thicknesses are different so this exercise is made with other dimensions and results are not be compared.

Figure VC0-2 Cantilever and proof mass

Auburn University device (Ref 1)

Tutorial Overview

This tutorial is organized into three exercises, which demonstrate various techniques:

Exercise 1: Technology setup

- how to start a project
- how to add material to a Material Property Database
- how to create a suitable process

Exercise 2: 3D modelling

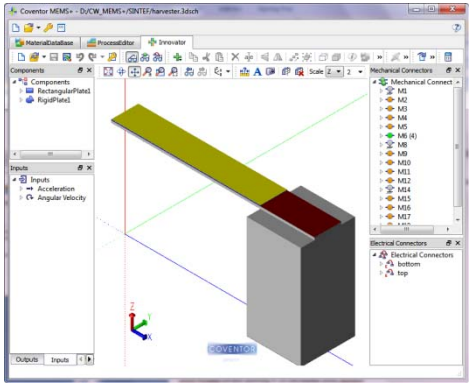
- how to draw a layout
- how to create the 3D MEMS
- how to mesh it

Exercise 3: Simulations in Analyser

- how to run a piezoelectric modal analysis
- how to run an harmonic with load

Energy Harvester design in **MEMS+**

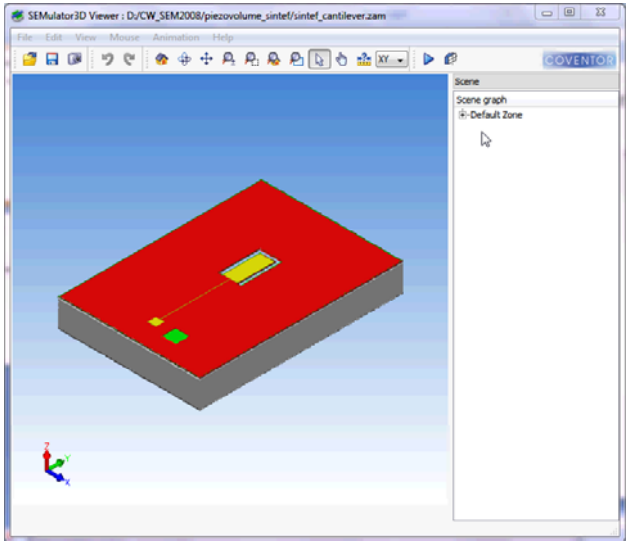
Advanced user manual



Tutorial Overview
Exercise 1: Technology creation
how to use a design kit
Exercise 2: Design in Innovator
how to parameterized dimensions
how to create the 3D MEMS with components
how to connect components
How to define boundary conditions
Exercise 3: Simulations in Cadence
how to run a modal analysis
how to run a DC sweep
how to build a circuit around the MEMS and run harmonic simulations

Cantilever virtual fabrication in **SEMulator3D**

Slide show and live exercises



All materials are available for distribution

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Deposition of PZT thin films in 2008-2009

	$-e_{31,f}$ [C/m^2]	Relative permittivity. e_r	Dissipation factor, tan d	Main bottleneck for high volume
CSD	12-18	1100-1600	~0.03	Throughput
Sputtering	~4-10	700-900		Quality

- CSD: High quality, throughput must be ensured by automation
- Sputtering:
  - Multi target DC reactive sputtering: low throughput
  - Single oxide target RF sputtering: higher throughput, but still too low quality

Deposition of PZT thin films in 2011

	$-e_{31,f}$ [C/m^2]	Relative permittivity. ε_r	Dissipation factor, tan δ
CSD	›14	1100-1600	~0.03
Sputtering	›14	700-1400	~0.03
PLD	›14	same	same

Status PiezoMEMS 2011:

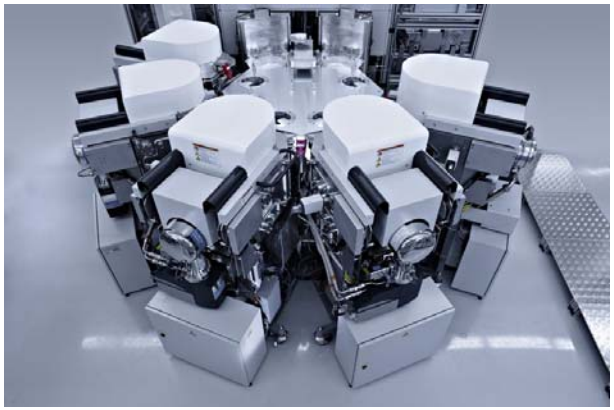
- $e_{31,f}$ jumping up.
- Very high influence from measurement and poling procedure

A new standard for characterization of PZT thin films is needed

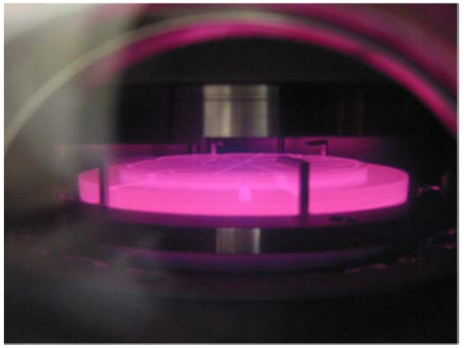
Separate talk by Oerlikon today 0945

Deposition tools – sputtering

- New hot chuck sputtering add-on for Oerlikon's Clusterline 200 II for in-situ sputtering of PZT
- Throughput goal
  - 3.6 wafers/h·µm (60 nm/min) on 200 mm wafers
- Performance goal
  - $e_{31,f}$ ~ -14 C/m^2
  - Thickness uniformity < ± 5 %



Oerlikon Systems Clusterline 200 II

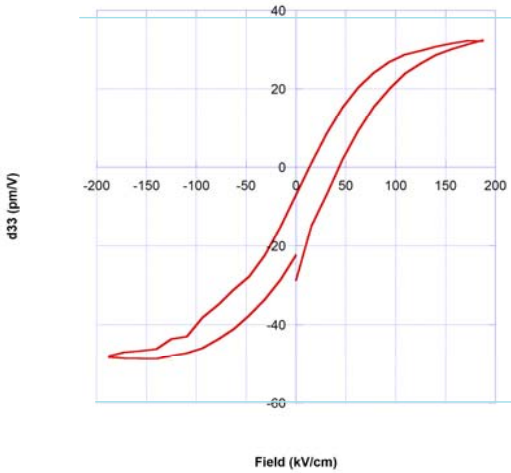


Hot chuck during sputtering

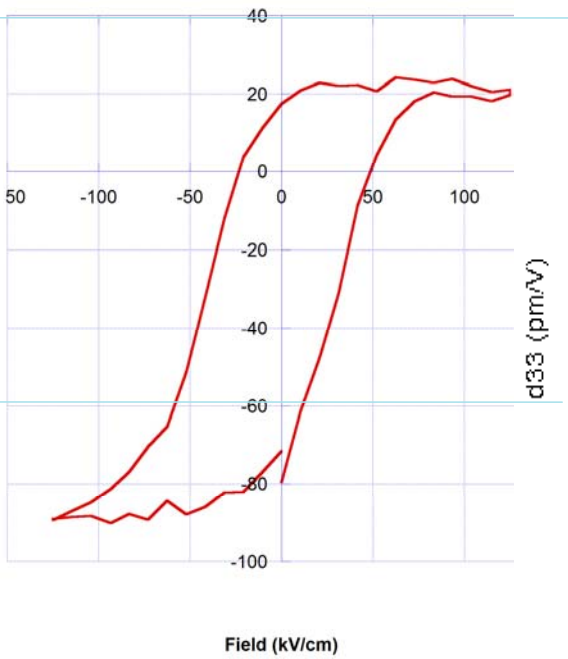
Sputtering – progress on 150 mm

- $d_{33,f}$ = 100 pm/V
- $e_{31,f}$ = -7 C/m^2 after poling for 20 min at 150 °C under a field of 170 kV/cm

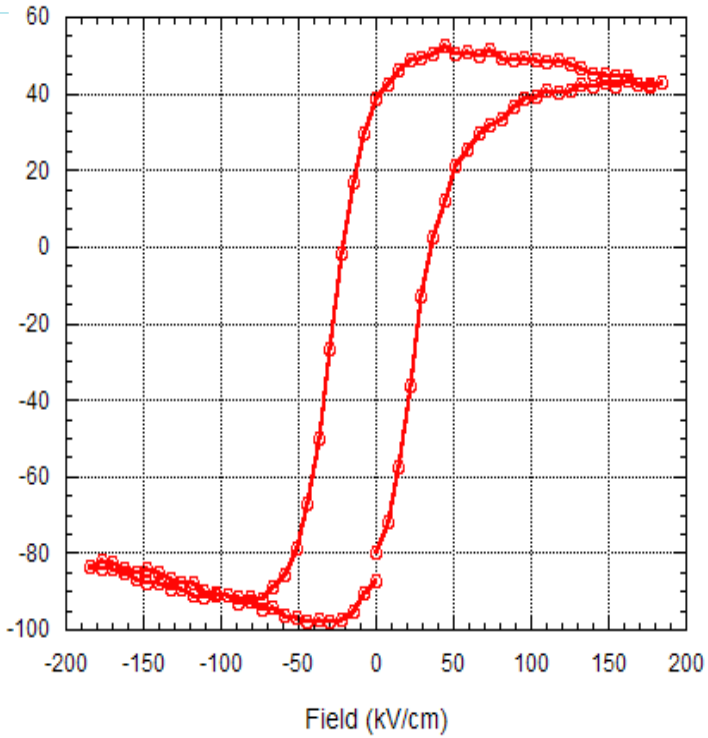
After 6 M



After 12 M

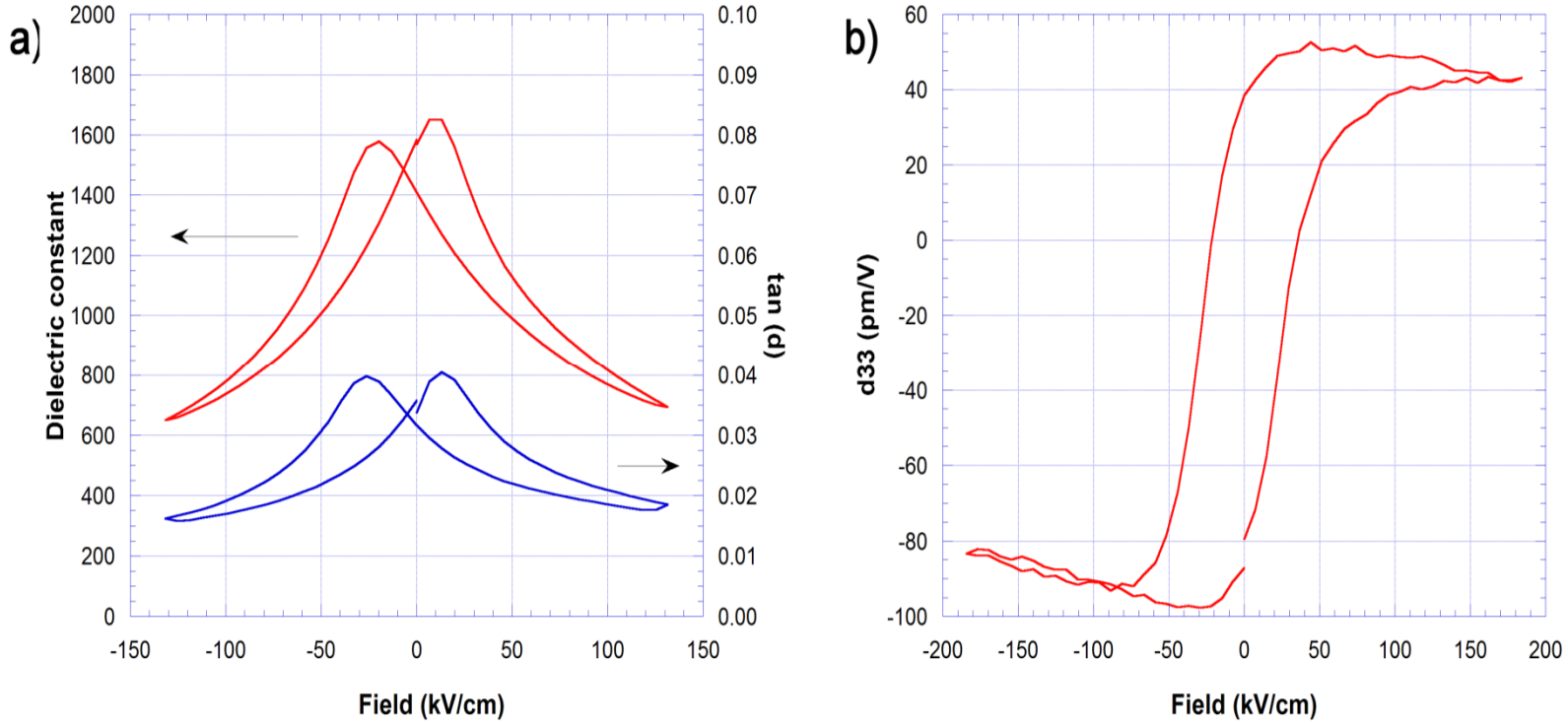


After 15 M



ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Sputtering – progress on 150 mm

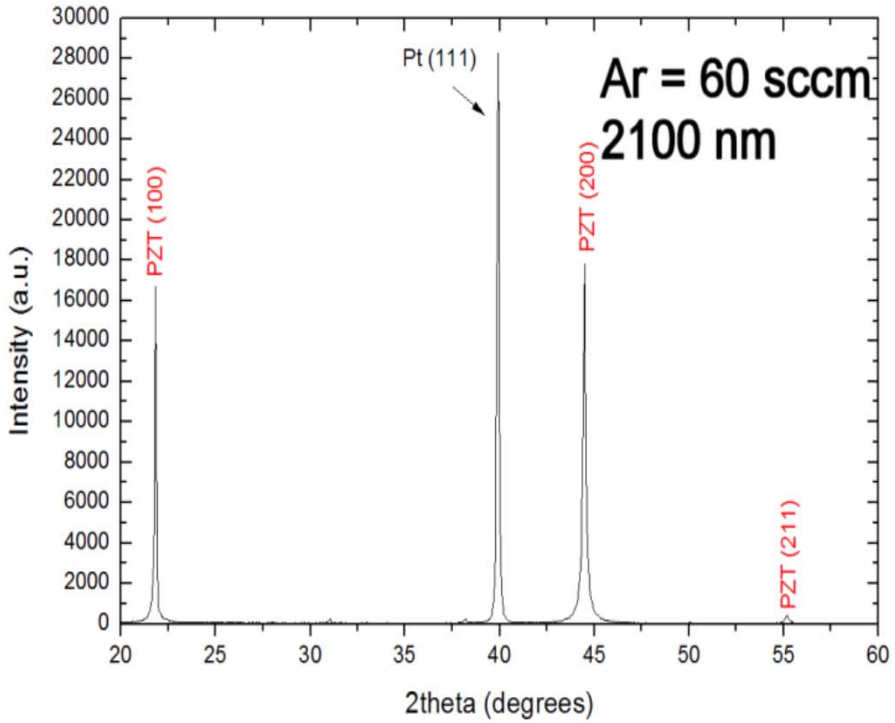


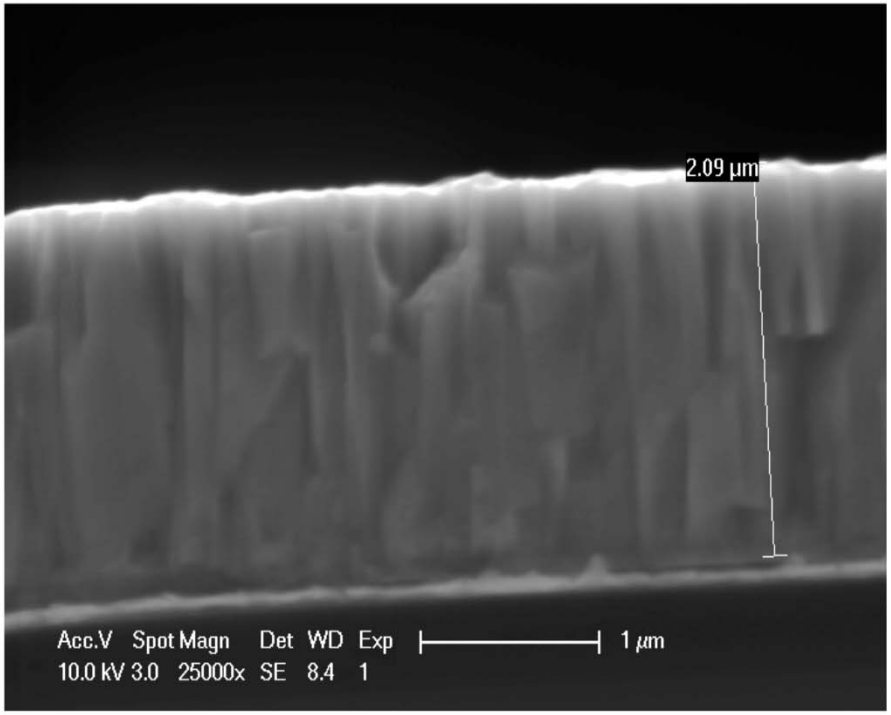
eps = 1500

$e_{31,f}$ = -7 C/m^2

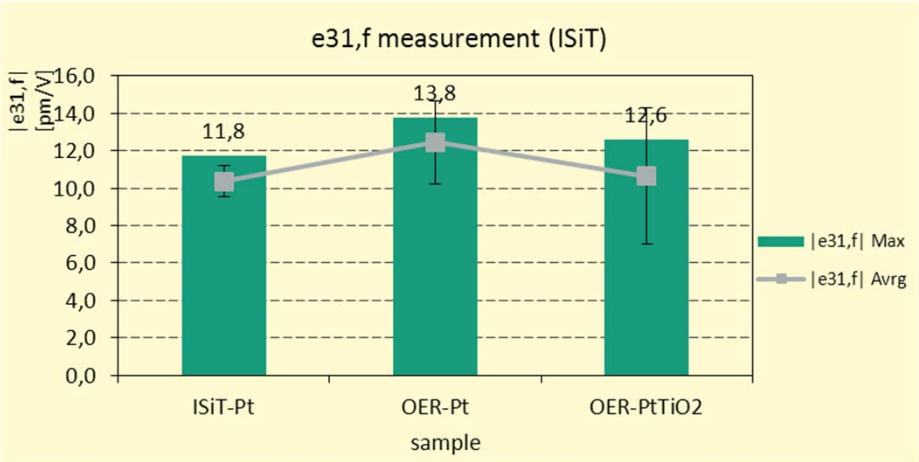
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

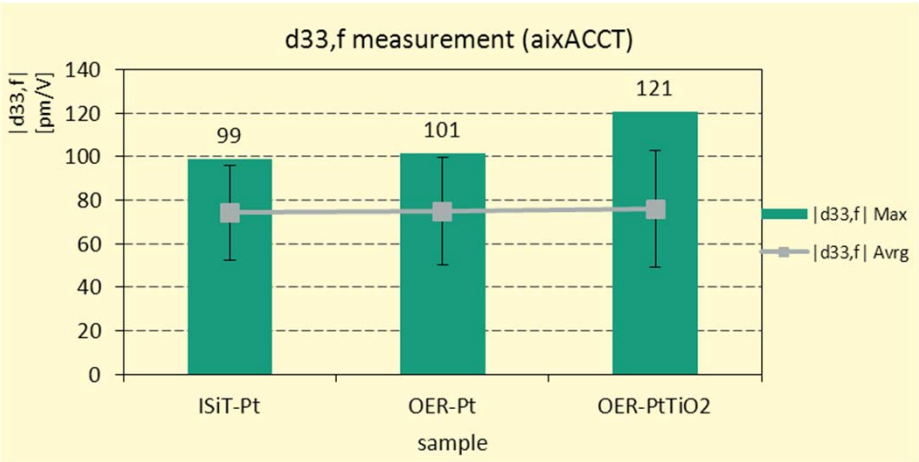
Sputtering – progress on 150 mm

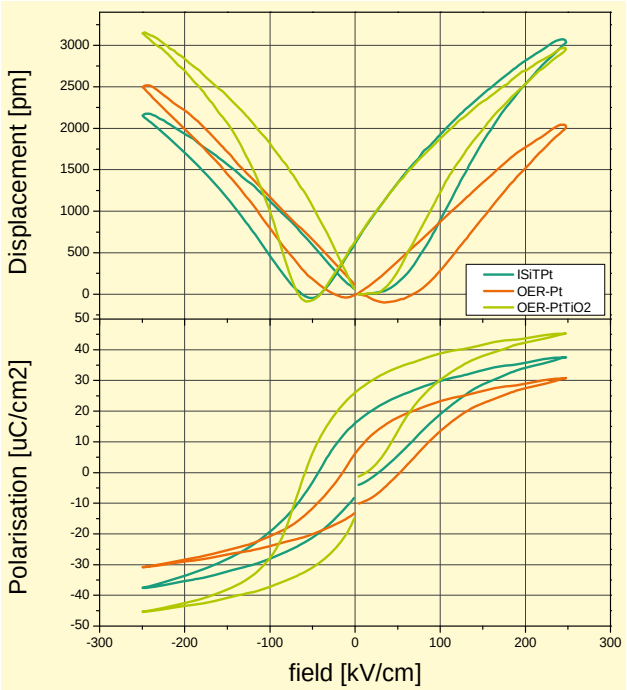




Properties of sputtered PZT on 200 mm

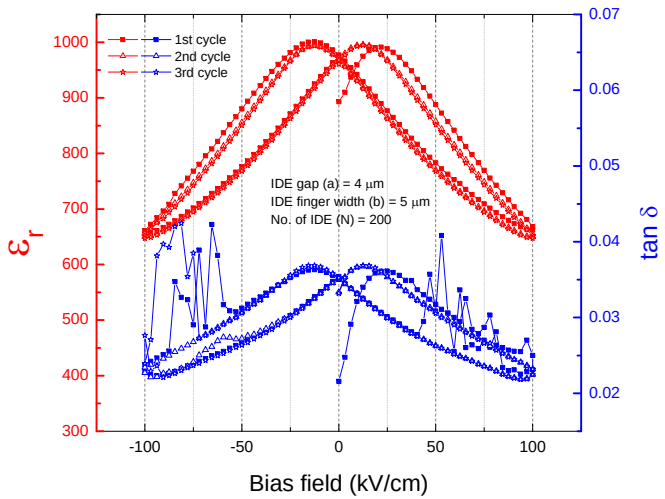


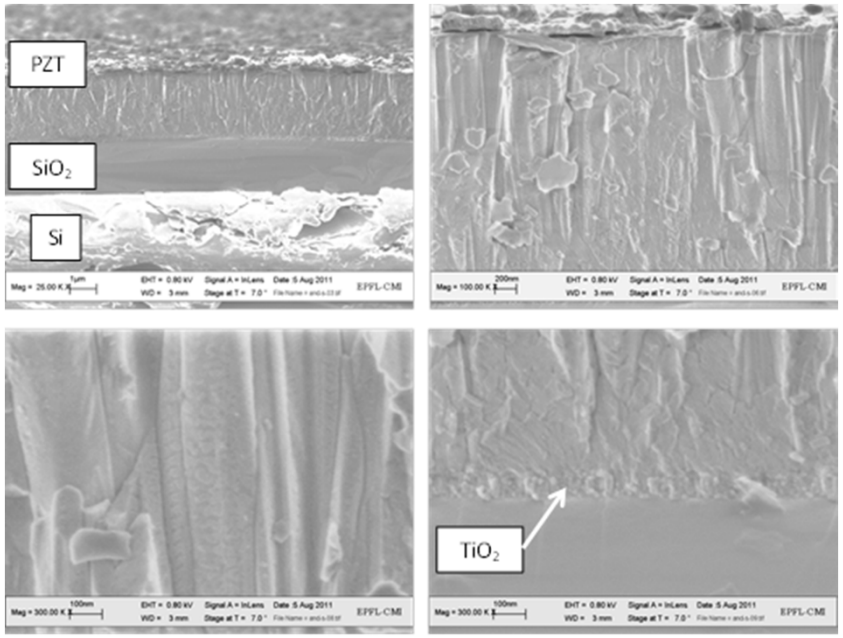




Sputtered PZT on bufferlayer for IDT electrodes

- Fresh result from last week
- e_{IDE} = 7 C/m^2 See poster P6





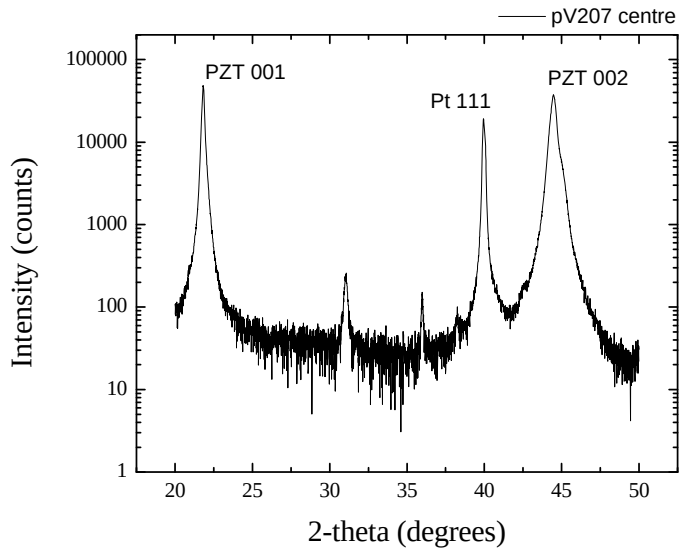
Deposition tools – CSD

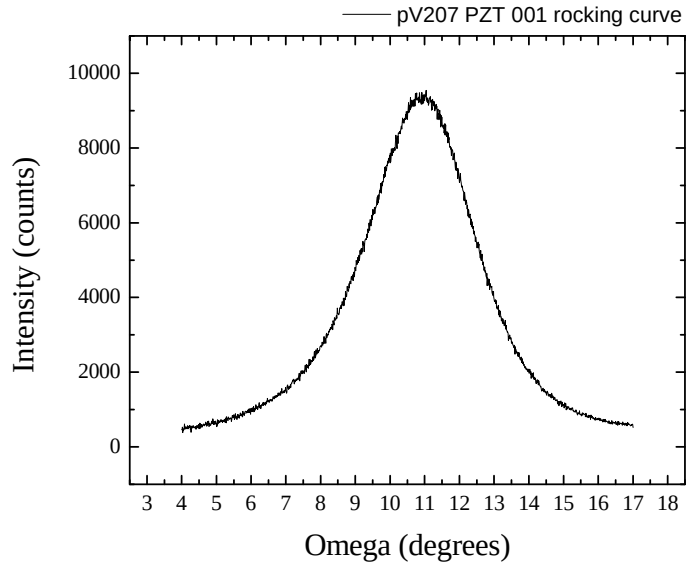
- Adaptation of Solar-semi cluster coater tool
- Throughput goal
  - 4 wafers/h µm on 200 mm wafers (67 nm/min)
- Performance goal
  - $e_{31,f}$ ~ -14 C/m^2
  - Thickness uniformity < ± 5 %

Solar-semi coating cluster

PZT deposition – CSD PZT quality

- Device run finished now in Sept. 2011
  - 2 µm PZT is 99,8 % (001) oriented on Pt electrode
    - ICSD #90700 as reference
  - Rocking curve of PZT 001 with FWHM of only 3,6 degrees.
  - PZT deposited on insulating buffer layer for interdigital electrodes
- New CSD processes
  - Thicker coating layers
  - Crystallization down to 500 - 550 °C
- New RTP process developed to accommodate increased thermal masses of thick wafers





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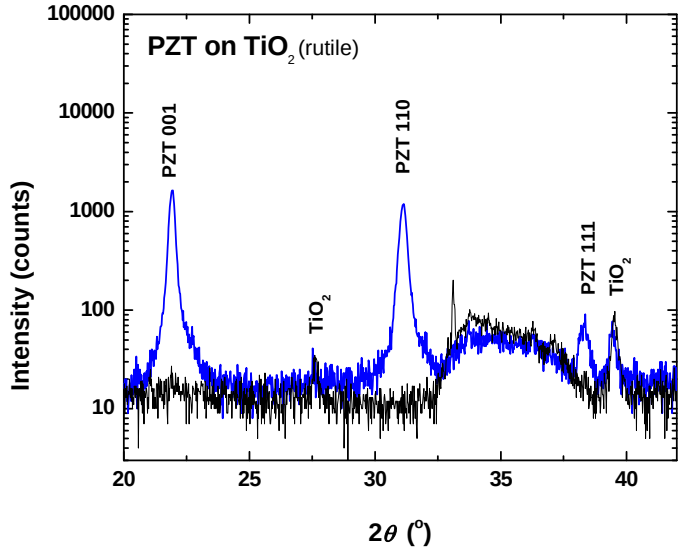
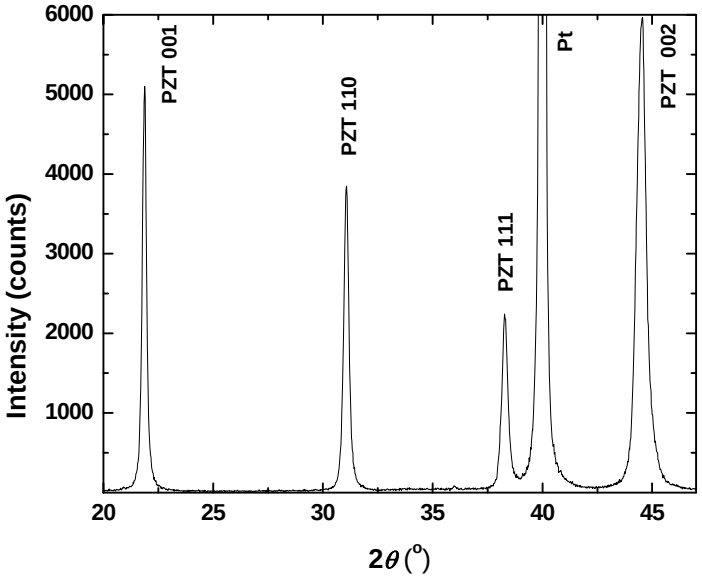
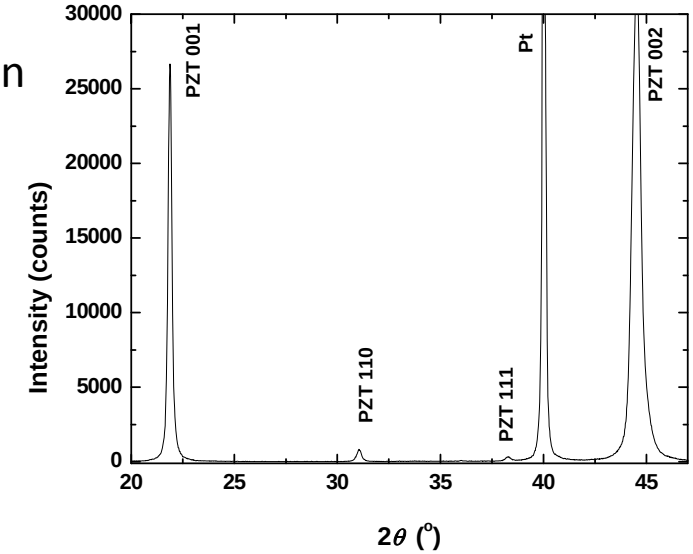
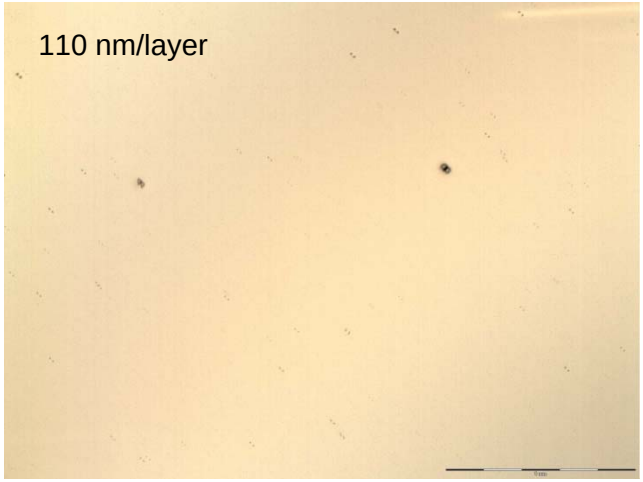


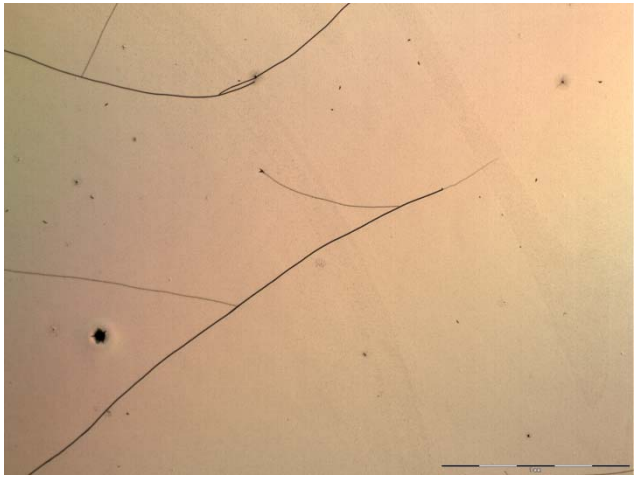


Improved orientation

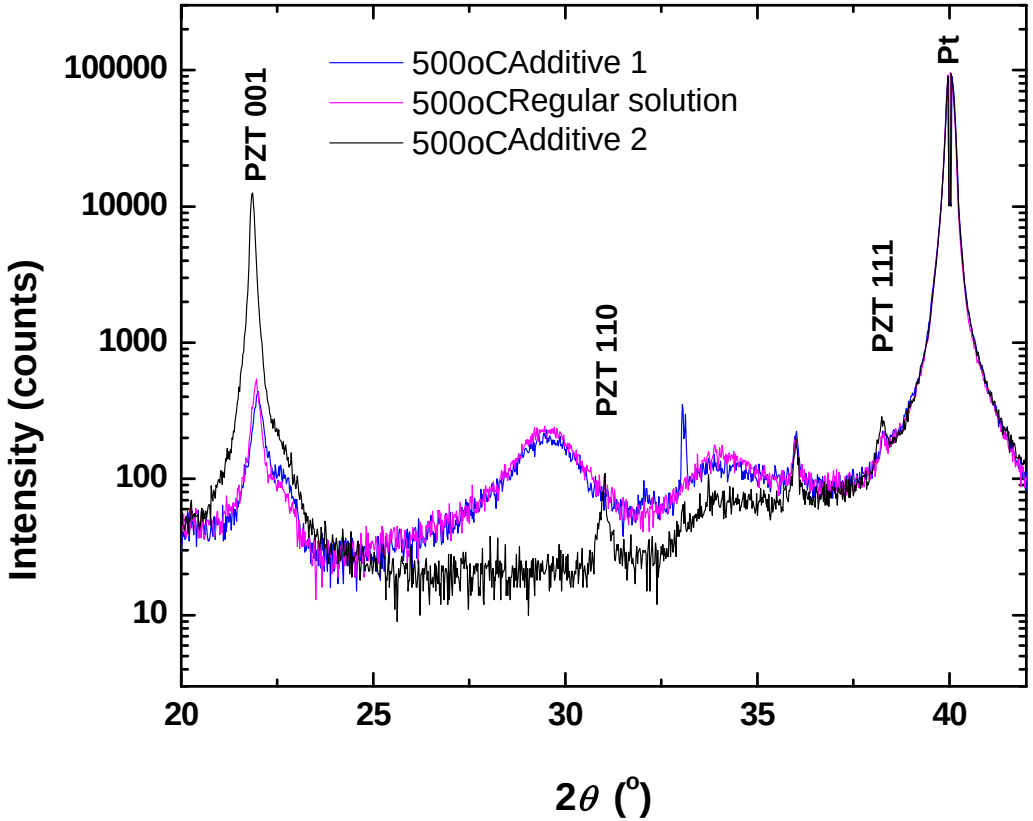




Improved orientation
Increased stress
Cracking



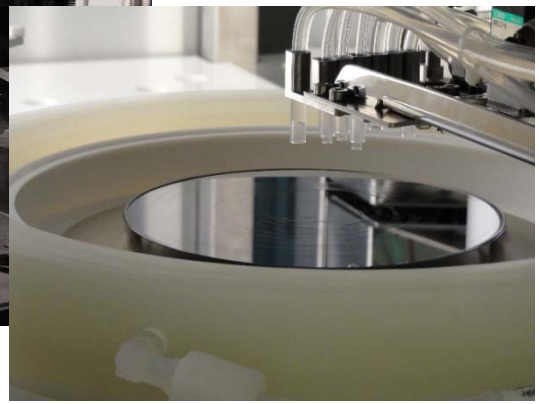
CSD PZT – lowering crystallization temperature



solarsemi GMBH

Automatic CSD tool development

Rotating covered chuck and media arm



Wafer on chuck with media arm

solarsemi GMBH

Coater module

- **Dynamic Balanced System** (Patent pending)
  - eliminates substrate vibration, for best uniformity and process control

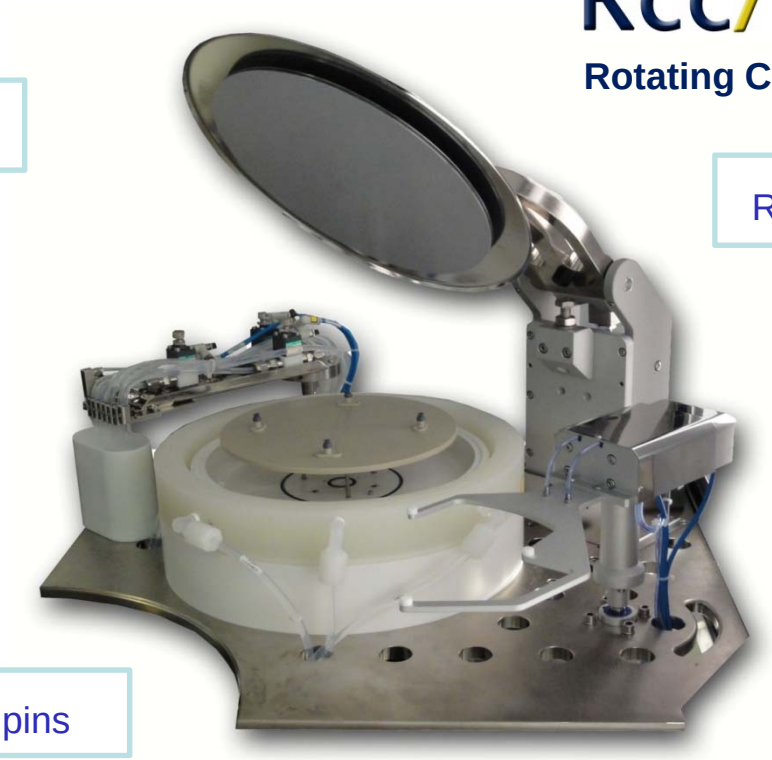
- **RTTC Features**
  - Solvent saturated atmosphere
  - No turbulence around the substrate
  - Eliminates rotational corner effects
  - No contamination on the rotating cover from coating solution
  - Self cleaning basic-chuck by "Venturi"-effect
  - Chuck rotation after closing rotating cover
  - 100 % sealed process chamber assures best coating uniformity
  - Cover plate laminated with Teflon to keep away external particles

solarsemi GMBH

Spin-coating-module incl. RCCT

RCCT™

Rotating Covered Chuck *T*echnology



Media arm

Inlay

Basic chuck

Process bowl

Lift pins

Rotating cover

Wafer handling Booster

Process bowl rinsing

How to do quality monitoring?

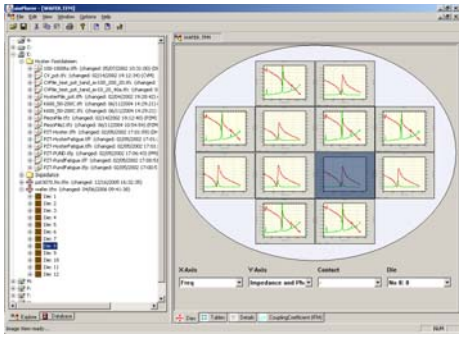
Method	Information retrieved	Suitability for high volume piezo thin film quality monitoring
In-situ XRD	Structure/texture/ morphology	No 1:1 correlation between e.g. rocking curve and piezoelectric performance
Ellipsometry	Thickness/refractive index	Only thickness
Electromechanical	Piezoelectric coefficients/ε_r	Wafer must be processed to extract the coefficients

Separate talk by aixACCT Tuesday 10:20

In-line quality monitoring

- Indirect estimation of $e_{31,f}$ from $d_{33,f}$ and ε
  - Needed resolution for thin films <10 pm
  - Laser interferometry
- Accuracy
  - Better than 4 % of real $e_{31,f}$
- Throughput
  - 10 wafers/h
- Automation of measurements through electrode mask layout
  - Parameter/coefficient tracking

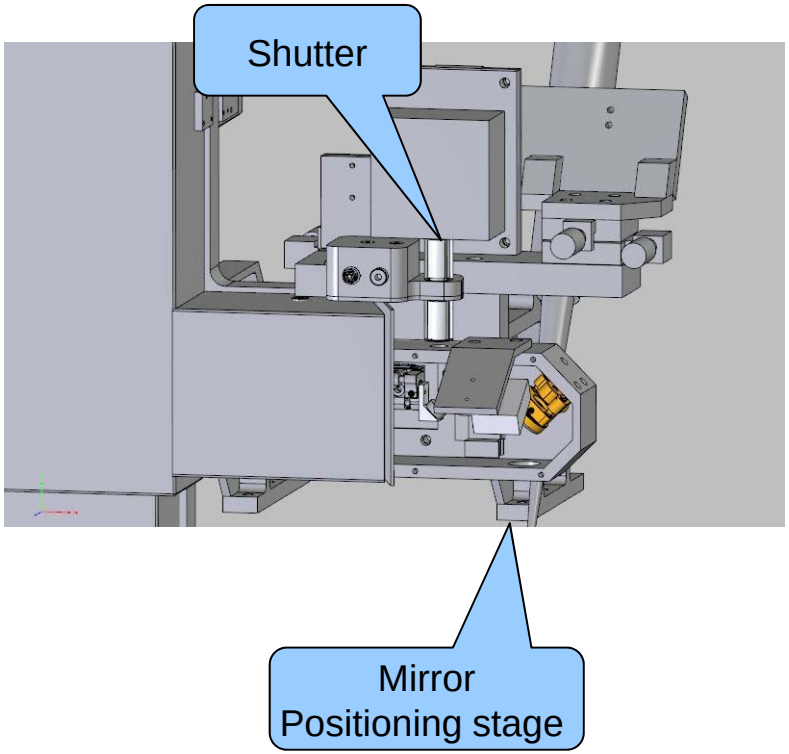
aixACCT double and single beam laser interferometer

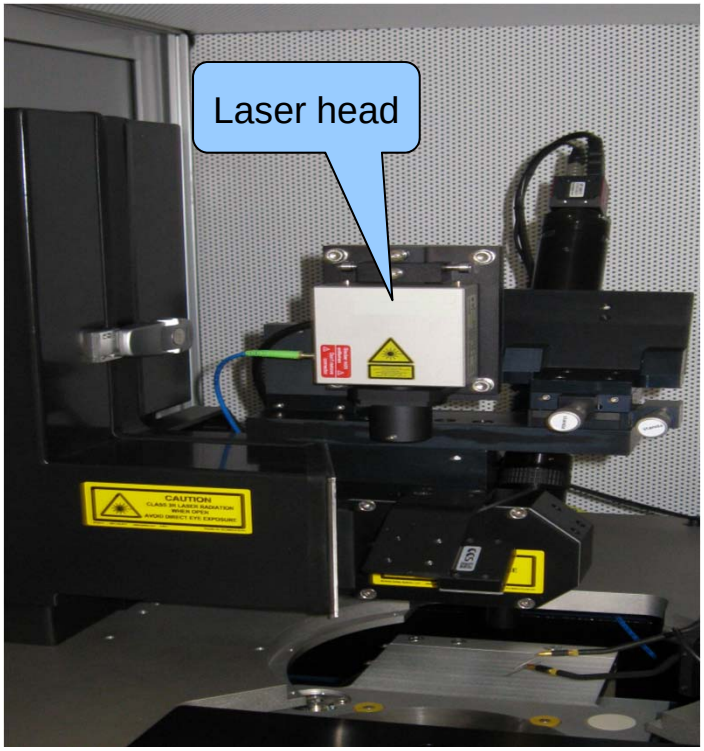


aixPlorer data management and analysis software

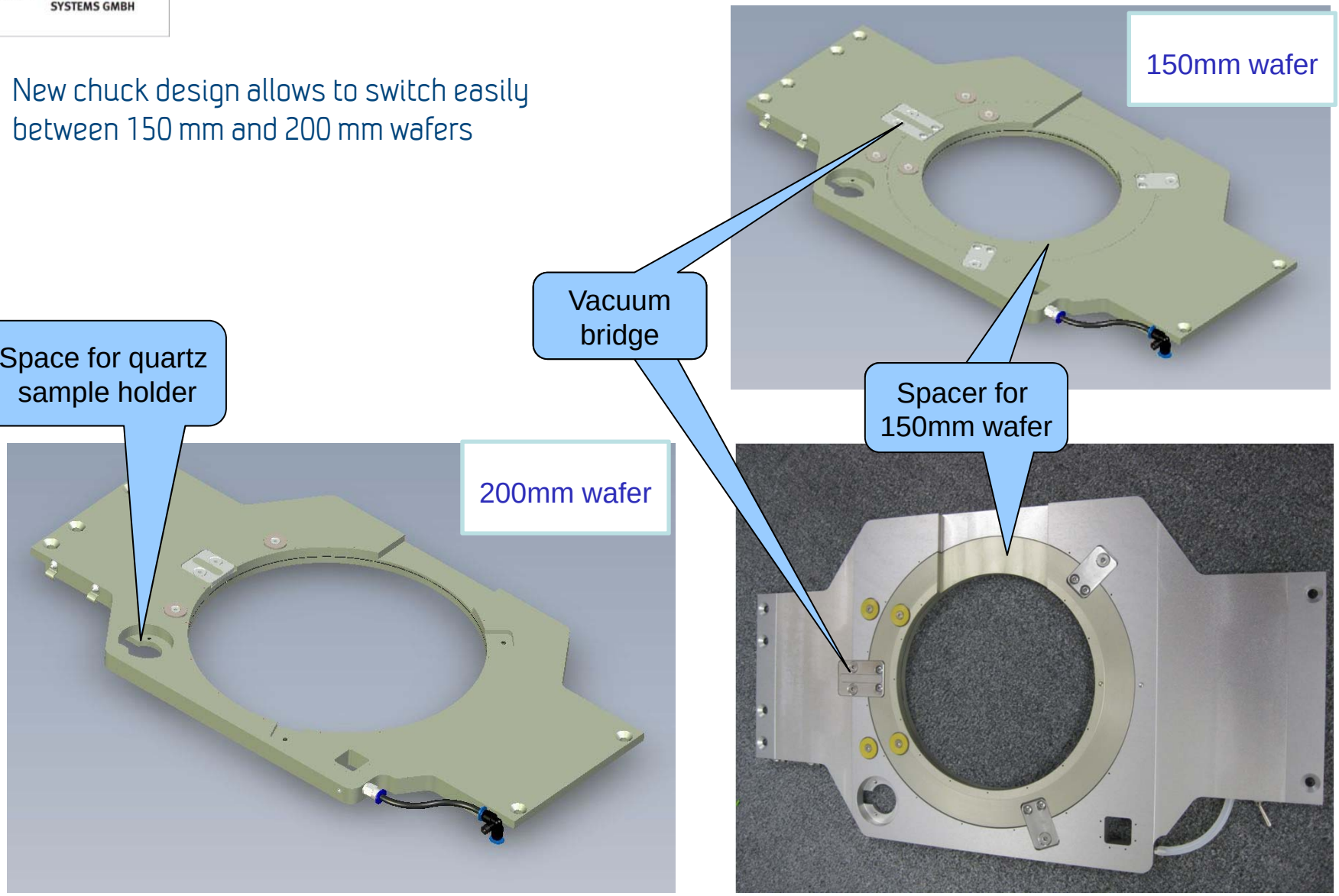
Measurement stage

- DBLI/SBLI automatic change between both modes automatically
- Air damping and active damping system have been evaluated according to vibration environments
- Design of the machine according to semi standard

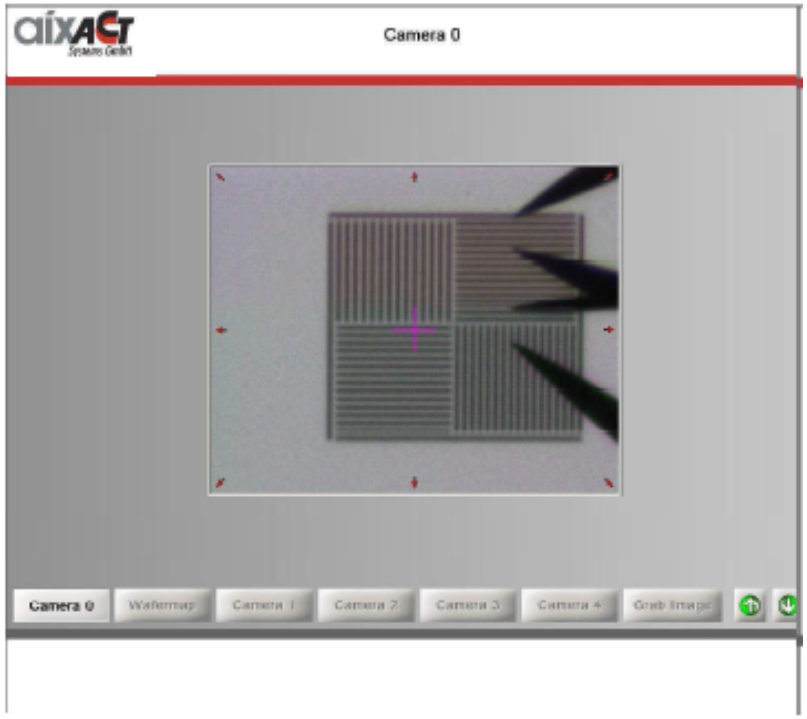


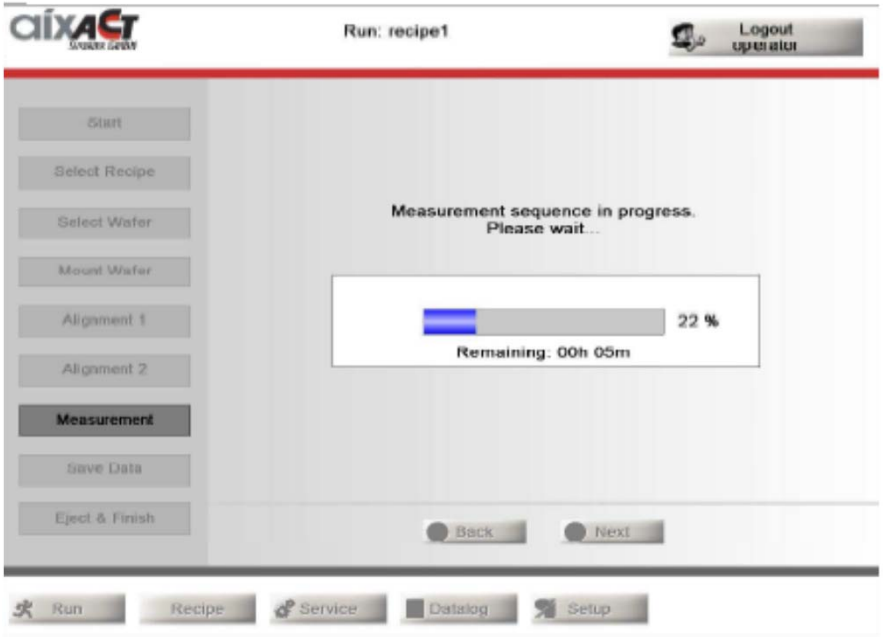


New chuck design allows to switch easily between 150 mm and 200 mm wafers



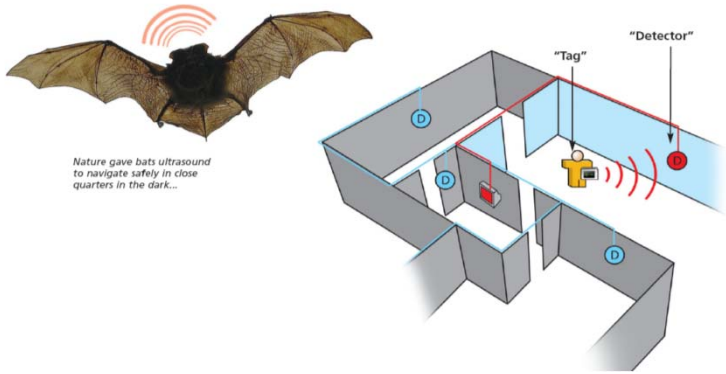
Measurement software





piezoVolume end users

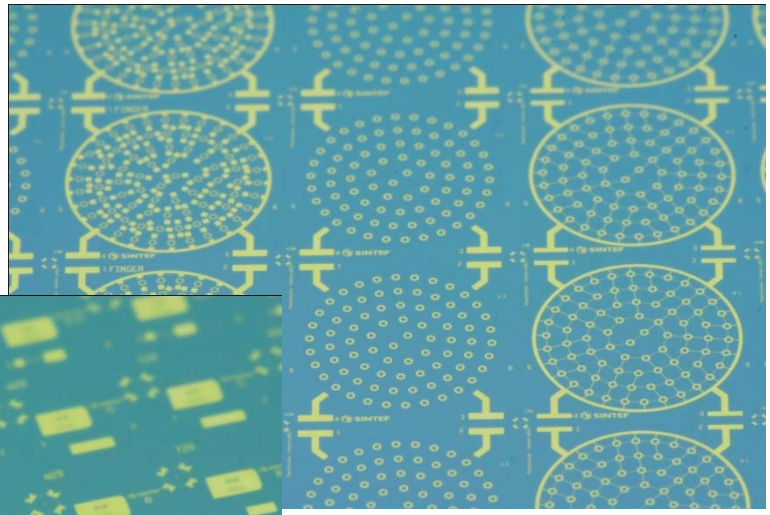
- Sonitor
  - Microphones for ultrasonic indoor positioning



- Océ Technologies
  - Ink jets

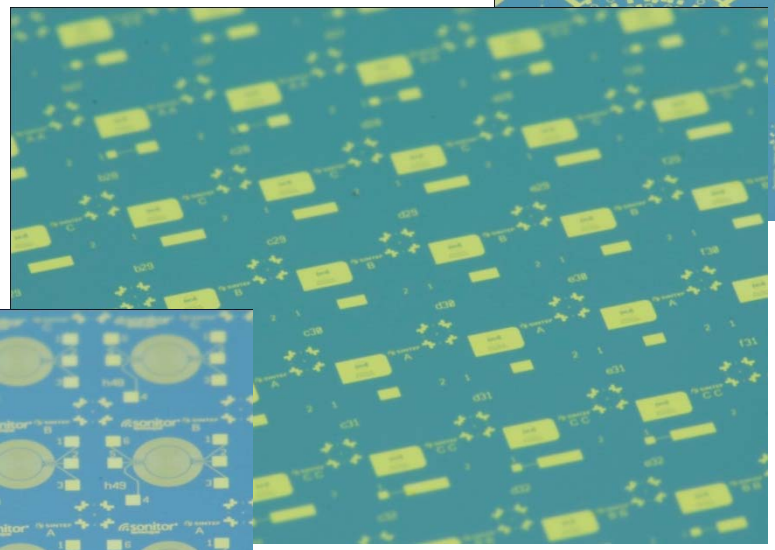
- VERMON
  - pMUT for medical ultrasound

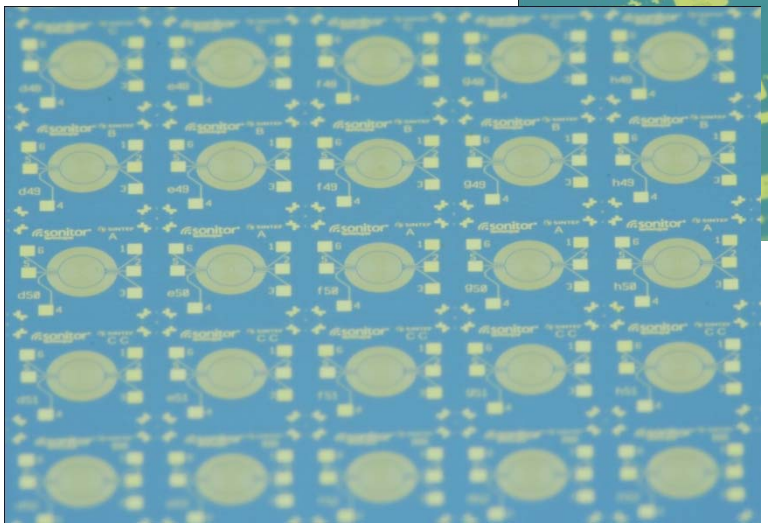
piezoMEMS processing



Vermon pMUT device

Océ ink-jets



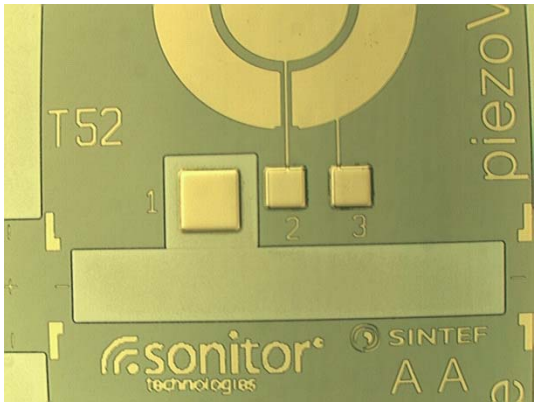


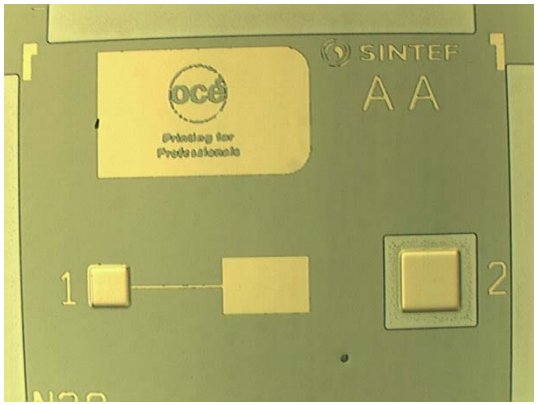
Sonitor microphones
(Interdigital electrodes)

piezoMEMS devices – dielectric insulation and cross routing

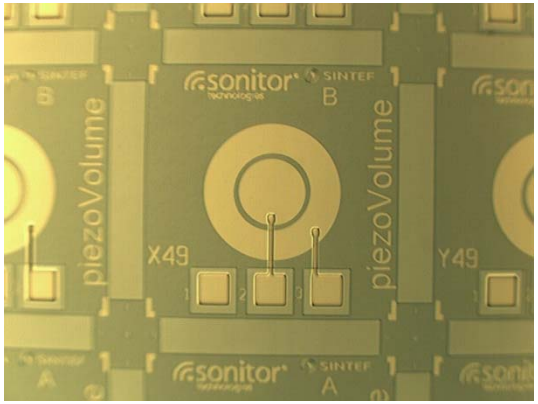
- Patternable dielectric layer
  - Reduction of stray capacitances
  - Enable cross routing

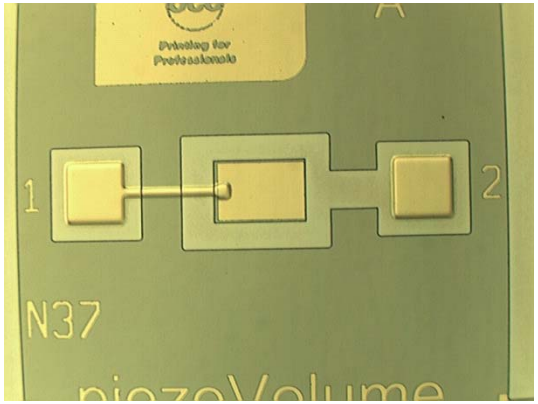
Standard design



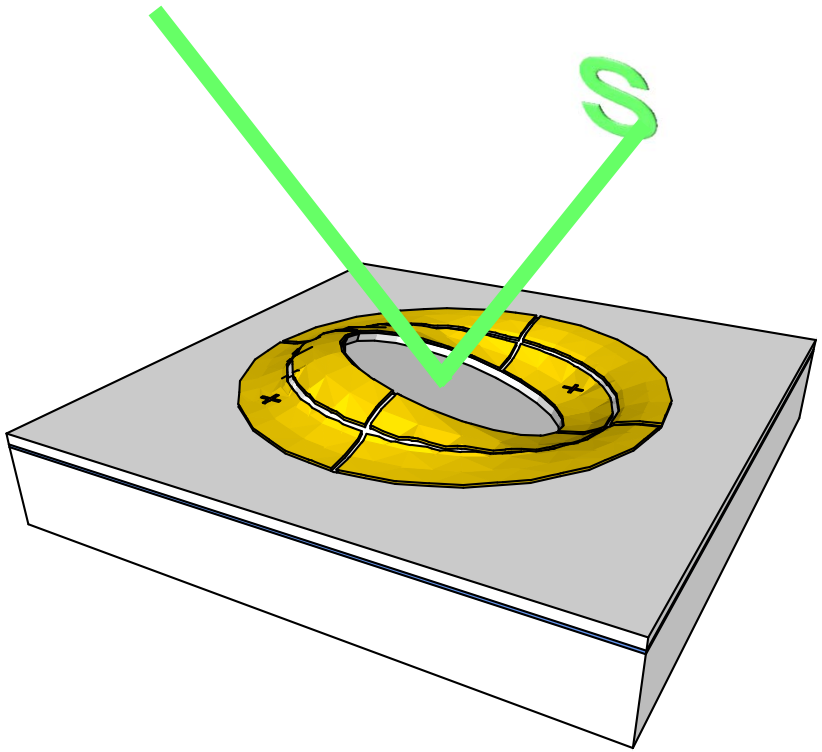


Design enabling routing over dielectric





2D micromirror for laser beam scanning



- Static tilt possible (non-resonant)
- High frequency (~10kHz)
- Planar (~10nm peak-to-valley)

Thor Bakke et al., SINTEF MiNaLab

piezoMEMS competence centre

- The competence centre aims to act as contact point for interested parties and covers the whole production process for piezoelectric microsystems
  - Long experience
  - Experienced project partner

  - Deposition process and tools for high-performance PZT thin films on silicon wafers
  - Modelling software specifically for piezoMEMS
  - Modelling of device ideas and design assistance
  - Evaluation of alternative processing routes
  - Testing services and sophisticated testing equipment
  - Manufacturing of prototypes
  - Small scale production using 150 mm wafers (now) and 200 mm wafers (soon)

www.piezovolume.com
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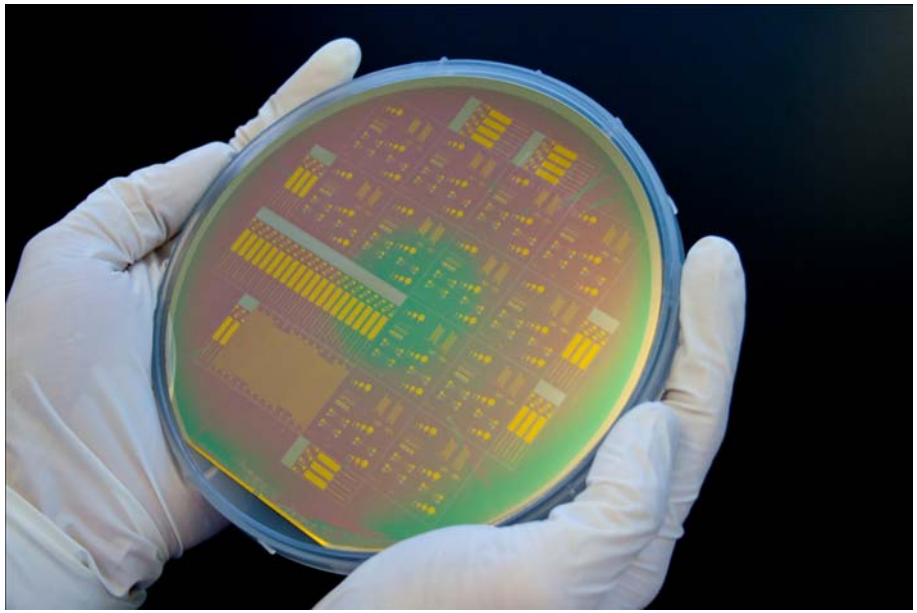
Project status

- Project started Jan 1st 2010
- Modelling tools
  - piezoMEMS PDK for Coventorware available from COVENTOR
  - Further developments in 2011 – 2012
- Deposition tools
  - Very promising results. Much more to come in 2011 – 2012
- In-line quality monitoring tool
  - Tool qualification finished
  - Further developments in 2011 – 2012



Check status at

www.piezovolume.com

Acknowledgements

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Thank you!