N-type silicon solar cell with Al back junction: results and modeling.

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Abstract

We present results on n-type silicon cell process development based on the Al-back junction concept using low cost fabrication techniques. Excellent results have been obtained on floatzone silicon wafers with efficiency in excess of 16.4%. Moreover, model calculations allow us to identify the potential for further enhancement of the cell efficiency above 17.5% by improving front surface passivation. After some optimization, high efficiencies may be conceivable on n-type multicrystalline substrates as well.

Introduction

More than 90% of the commercial solar cells fabricated so far are based on p-type doped silicon material that was received from the electronic industry. Nowadays over 80% of the produced solar cells have a homogeneous emitter, a PECVD-SiN layer as antireflective coating, and screen printed contacts on both sides. For the backside, an aluminum paste is used to create a back surface field during the contact co-firing. Currently there is much interest in the development of low-cost industrial cell processing based on n-type (multicrystalline or monocrystalline) silicon wafers. This interest is based on several developments and findings, such as:

- High carrier lifetimes in n-type multicrystalline wafers, often significantly higher than in p-type wafers.
- Theoretical and experimental evidence for less recombination-active defects in n-type silicon [1].
- Tolerance of n-type silicon to high temperature processing with respect to p-type silicon [2].
- Shortage of silicon feedstock for the PV industry, and an unused potential supply of n-type silicon waste.
- New materials (ribbons, metallurgical feedstock) for which the above aspects favor n-type doping.
- Need for technology development towards very thin wafers and high cell efficiency, for which n-type silicon based solar cells may have advantages.

A few solar cells concepts based on n-type Si materials are under investigation. One of these concepts is the Al back-junction cell.

In this paper we present results on n-type cell process development based on the Al back-junction concept (also known as phostop, as introduced by Ebara [3]). The phostop represents a fast way, from industry side, to move from p-type to n-type substrates because of the possibility of maintaining the same process sequence. The only difference is that during the phosphorus diffusion step a front surface field is created instead of an emitter and during the contact co-firing the aluminum back junction is formed. Therefore this process has received much attention recently, on a process similar to the one we present here [4, 5] and on smaller size lab process [6, 7]. We developed the cell process on 148.5 mm^2 Float Zone (FZ) n-type monocrystalline silicon wafers, but results on 156.25 mm^2 industrial n-type multicrystalline silicon (mc-Si) wafers are also presented.

Cell Fabrication

The cell process we used is based on in-line processing for diffusion, co-firing, and on process steps which can be industrialized. The rear junction as well as the front surface field (FSF), anti-reflection coating (ARC), and the metallization, are based on industrial standard n^+np^+ process, as shown in Figure 1. It starts with a wafer thinning [8] to about 150-180 μm followed by an isotexture etch of the surface. Then the front-surface field is formed by phosphorus diffusion in an infrared conveyor belt furnace from a spin-on source, resulting in 50-55 Ω/sq. front surface field. After phosphorus glass removal the PECVD SiN anti-reflection coating was deposited on front, followed by rear side etch and edge isolation [5]. Subsequently, the silver grid was screen-printed on SiN front side, followed by screen-printing of Al on the whole rear side of the cell. Both contacts were co-fired in an infrared conveyor belt furnace, thus forming also the back junction.

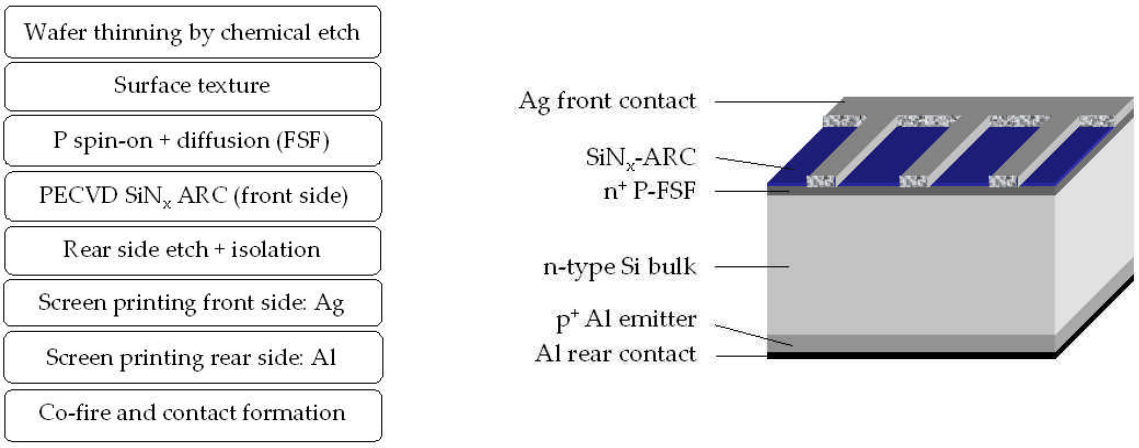

Figure 1. Process flow chart (left) and the layout of Al back junction solar cell (right).

Results and discussion

Table 1 summarizes the solar cell parameters of the best results obtained for mc-Si and FZ substrates. The highest efficiency of monocrystalline substrates is obtained for higher substrate resistivity (it is in fact nearly identical to the efficiency reached by Kopecek et al. [4] on similar substrates and with slightly different cell process). This is in agreement with model calculations [4,8], which show that, in order to benefit from the full potential of this type of solar cells, the wafer resistivity should be higher than 10 Ωcm (with a thickness of less than 200 μm). On the other hand it is important to know what limits the efficiency at lower substrate resistivity, especially for multicrystalline substrates. To understand this, we have investigated the internal quantum efficiency (IQE) of the cells from Table 1. Figure 2 (left) shows the experimental IQE (symbols) together with the PC1D fit (lines) using measured front doping profile and surface reflection, and assuming a constant Al doping profile for the rear junction. The relevant fit parameters for the modeling are the bulk lifetime and the front surface recombination velocity (SRV). Since for monocrystalline wafers the bulk lifetime is very high (>1 ms), it does not limit the IQE at lower wavelengths regime, where it is remaining completely determined by the SRV. The fit to experimental data reveals a SRV of $6(\pm1) \times 10^5$ cm/s for both monocrystalline wafers. Hence, the difference observed in IQE or in power conversion efficiency of monocrystalline wafers is accounted for only by the difference in their substrate resistivity. Such a good agreement between calculated and experimental data allows identifying SRV as the limiting parameter for solar cells efficiency based on monocrystalline substrates. Figure 2 (right) shows the model calculations of power conversion efficiency as a function of SRV. The starting point of this calculation was the experimental data of 16.4% efficiency cell. It is clear from the figure that an order of magnitude lower SRV would raise the efficiency above 17.5%. Work is currently under way to improve the passivation of phosphorus FSF of the Al back junction cell concept.

The bulk lifetime must be taken into account, however, when we analyze the current-voltage data of the multicrystalline wafers. The IQE fit of multicrystalline cell reveals the same SRV value as that obtained for monocrystalline cells, but with a considerable lower bulk lifetime of only 28 μs (as obtained from PC1D fit). It has been shown that the ratio of diffusion length and substrate thickness (L_d/d) must be higher than 2.5 to insure that the cell performance is not limited by the wafer quality [5]. Thus, to meet these conditions, the effective lifetime of the multicrystalline substrates must be higher than 130 μs. Hence, besides resistivity, the bulk lifetime is another important factor that limits the efficiency of n-type multicrystalline silicon solar cells with a rear side emitter.

Material	Resistivity [Ωcm]	Jsc [mA/cm^2]	Voc [mV]	FF [%]	η [%]
mc-Si	0.8	19.77	589	73.7	8.58
FZ	3.8	30.74	620	77.9	14.86
FZ	30	34.18	621	77.4	16.41

Table 1. Parameters of the best solar cells on n-type FZ and mc-Si substrates.

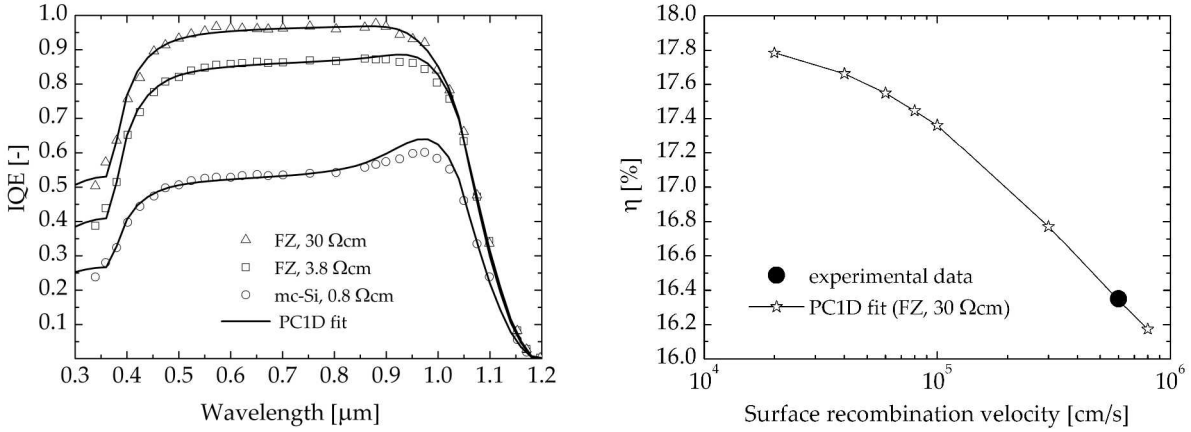

Figure 2. (left) Internal quantum efficiency (IQE) data of the solar cells from Table 1 (symbols) and its PC1D fit (lines), taking into account the measured front doping profile, surface reflection, wafer resistivity, and wafer thickness. The relevant fit parameters for the modeling are the bulk lifetime and front surface recombination velocity. (right) Calculated solar cell efficiency as a function of surface recombination velocity for an n-type FZ with a resistivity of 30 Ωcm. The parameters used in the calculation are those found by fitting the experimental data of Figure 2 (left). The increase in cell efficiency, due to an increase in J_{sc} and V_{oc}, is a result of a better front surface passivation.

It has been proven that a longer lifetime is obtained by increasing the wafer resistivity for multicrystalline substrates [9]; therefore, it would be important to know what could be the optimum resistivity to obtain the needed lifetime.

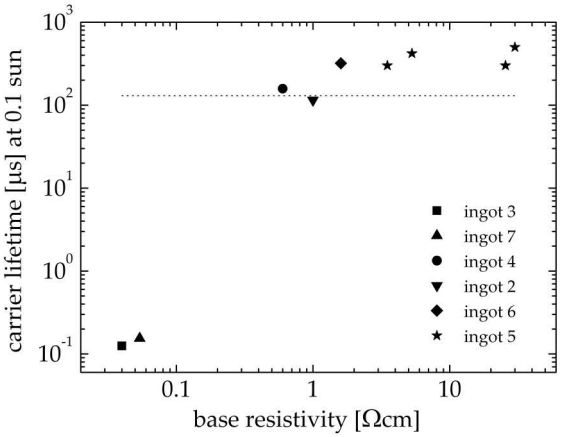

Figure 3. Effective minority carrier lifetime (symbols) as a function of base resistivity for various experimental n-type mc-Si ingots doped with As, Sb, or P (from their central parts). The effective lifetimes are measured using generalized Sinton QSSPC at an illumination level corresponding to 0.1 sun. The dotted line indicates the minimum lifetime required in order to guaranty that the cell performance is not limited by the wafer quality.

Figure 3 summarizes the effective minority carrier lifetime of various n-type multicrystalline ingots, measured using Sinton QSSPC at an illumination level corresponding to 0.1 sun. This illumination level approximately corresponds to the carrier density at the maximum power point of a cell. A sharp enhancement in lifetime, to values above 100 μs, is observed for wafer resistivity between 0.1 and 0.7 Ωcm. This is apparently in contradiction with the lifetime of 28 μs determined from the IQE of Figure 2 for the same base resistivity. However, the mc-Si wafer and cell suffer from spatially inhomogeneous lifetime distribution. Since the QSSPC method gives a locally averaged value for lifetime, the IQE lifetime, obtained by illuminating the entire cell, is the most realistic value. This is further supported by the light beam induced current (LBIC) scan of the mc-Si cell which shows a large variation in current density values on the whole cell, as is shown in Figure 4 (left). Partially

such an inhomogeneity was found to arise from a resistivity variation across the wafer, as shown by the resistivity scan of Figure 4 (right). We conclude that the lifetime inhomogeneity makes a significant difference in the solar cell performance [10]. Indeed, with higher resistivity and very homogeneous n-type mc-Si wafers, Kopecek et al. obtained cell efficiencies of 14.4% [4], and Cuevas et al. on small size 15.0% [6].

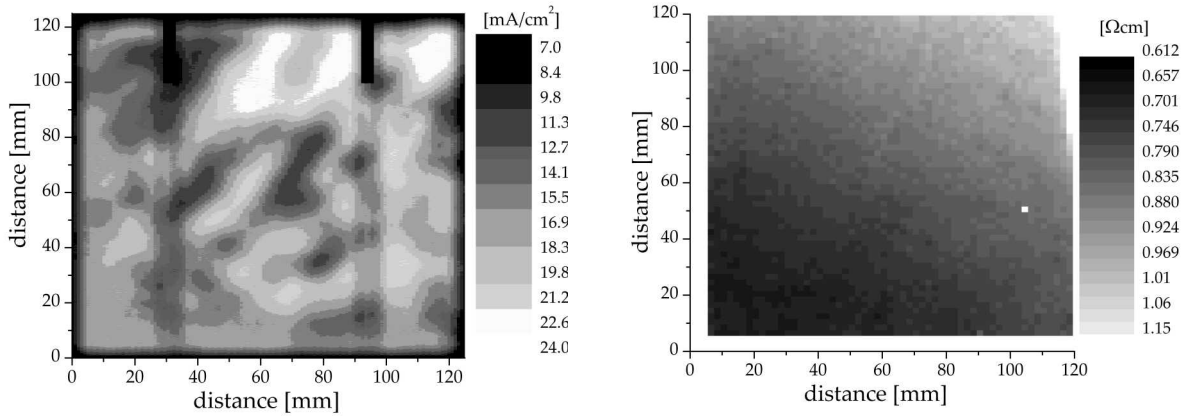

Figure 4. LBIC scan map (left) and bulk resistivity scan map (right) of the mc-Si of Table 1 (from the edge of the ingot). The resistivity scan was performed on an as-cut neighboring wafer.

Conclusion

We have demonstrated that a low cost process of fabricating n-type solar cells based on Al back junction concept leads to efficiencies up to 16.4% for monocrystalline substrates. Moreover, by improving the front surface passivation, efficiencies in excess of 17.5% could be realized, as demonstrated by our model calculations. High efficiencies may also be conceivable on n-type multicrystalline substrates after material optimizations, such as higher resistivity and increased lifetime homogeneity.

Acknowledgments

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