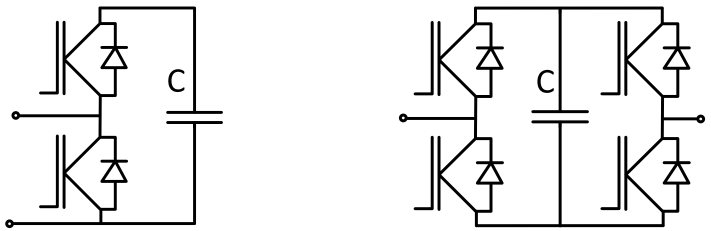
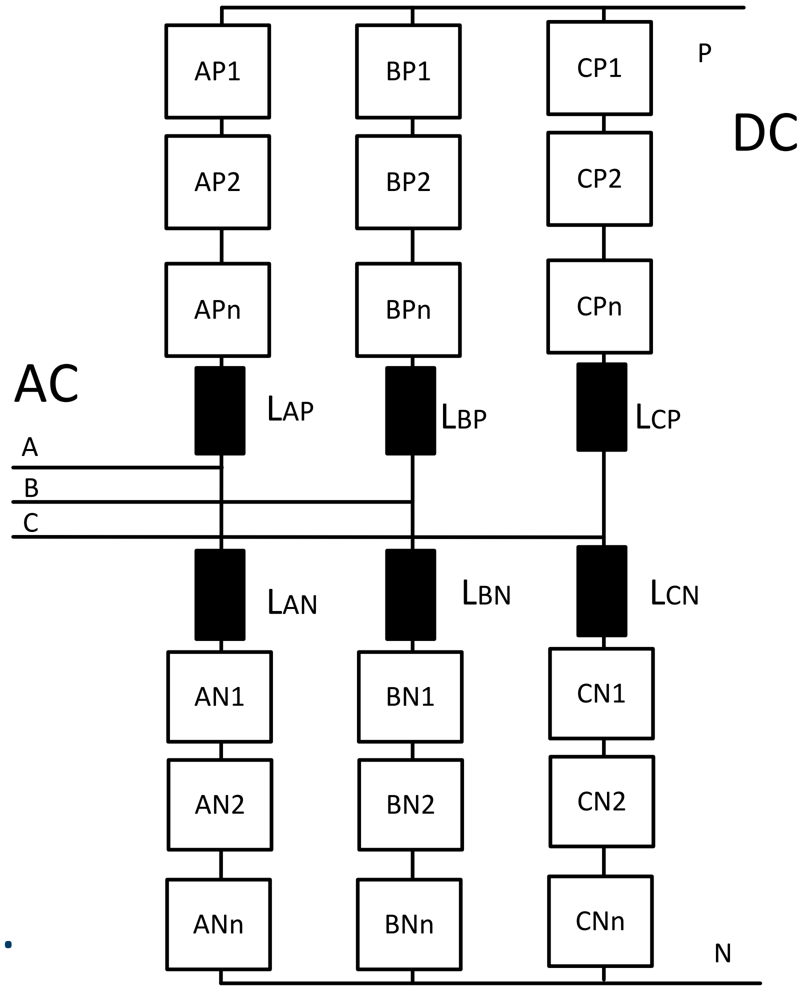
SCALE MODEL OF MODULAR MULTILEVEL CONVERTER

Kjell Ljøkelsøy

MMC topology



- Halfbridge or fullbridge cells
- Many low voltage cells: (~300 per arm)
- Energy for several periods in cell capacitors
- Good AC voltage control. Small voltage steps.
- Redundancy



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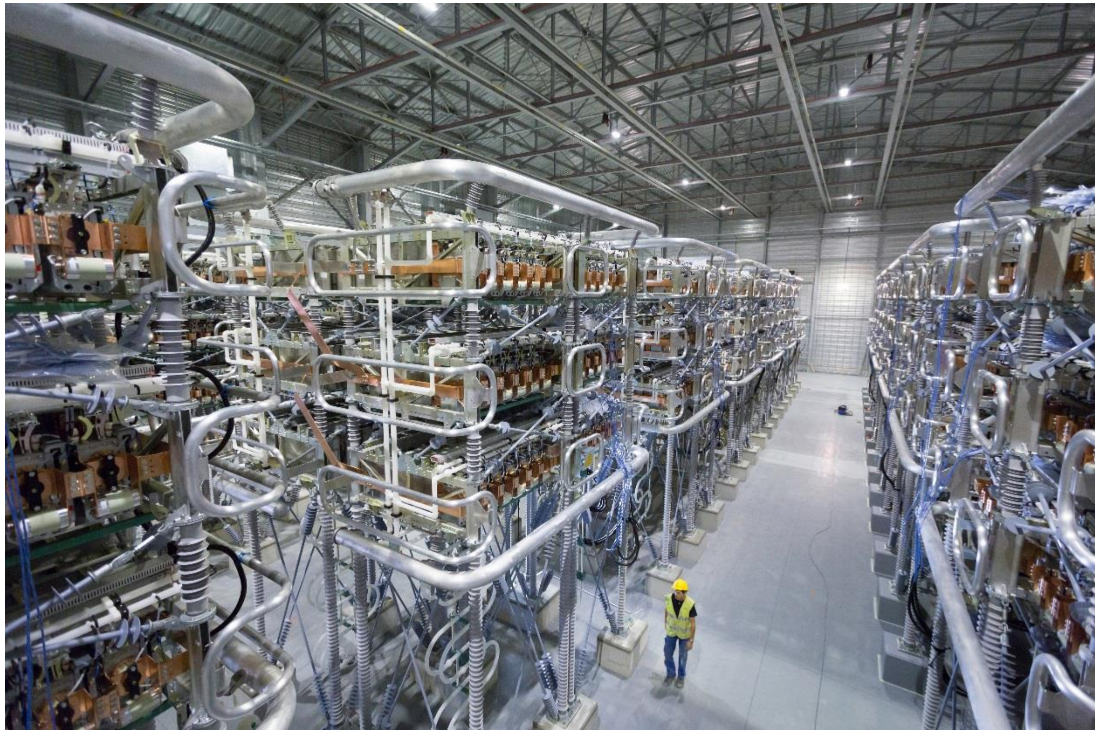
Why lab scale models?

- Many components, complex control.
  - Need for experience building.
- Testing on full scale systems not really feasible.
  - Potentially large consequences. Don't get access.
- Simulation models depends on model
  - Gives the answers you expect. Can miss unexpected aspects.
  - Assumptions and simplifications. May omit something important.
- Real converters contains most aspects.
  - Some adaptations and simplifications here too.



HVDC transmission link between France and Spain: HVDC Plus IGBT converter modules for 1000 MW. www.siemens.com/press".

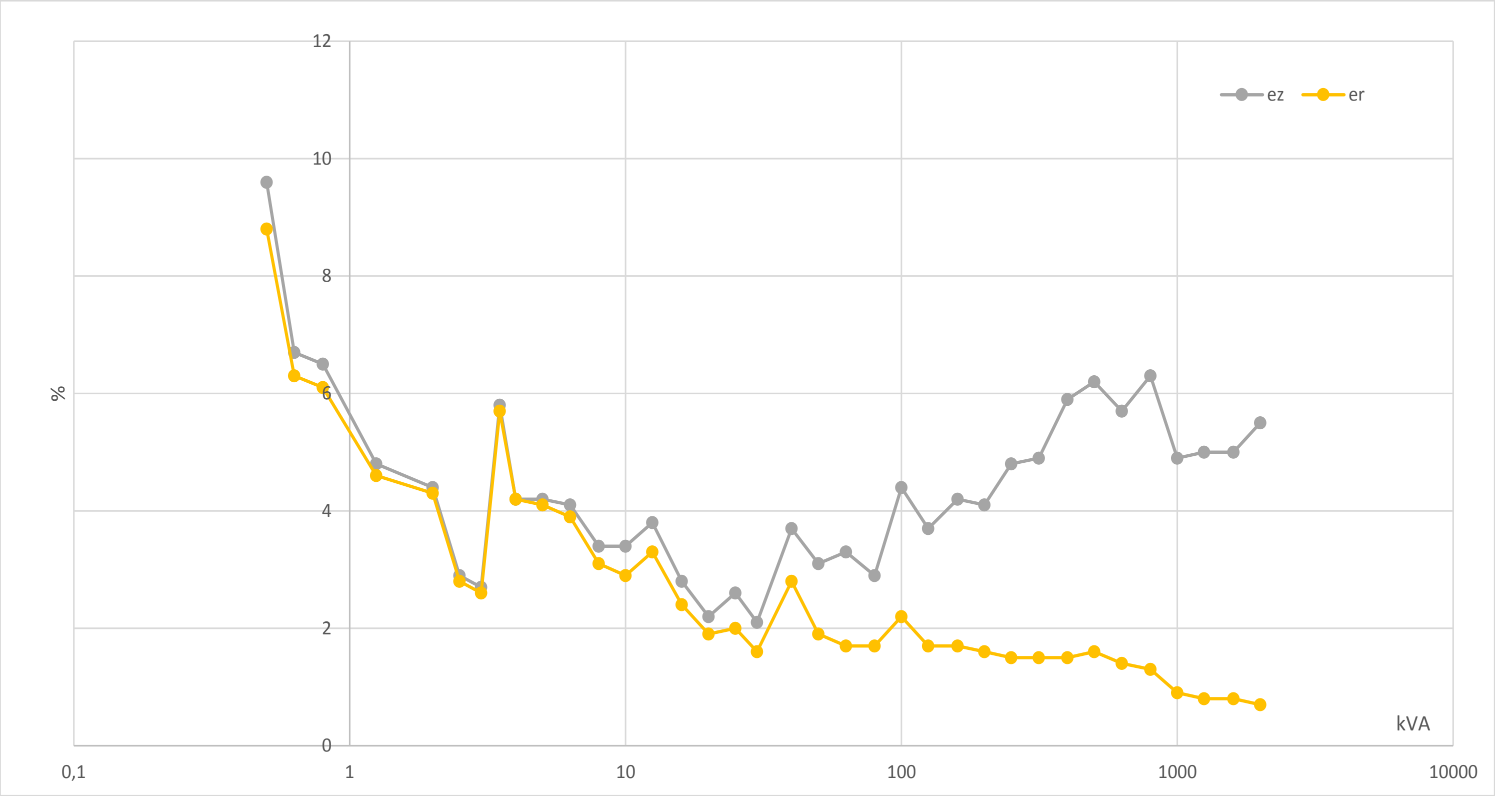
Choice of scale. Power level:

- Full scale: 1000 MW
  - Essentially unmanageable.
- Low power model:
  - Safe. Low cost. Ease of operation.
  - Can behave quite different from full scale reference
  - High series resistances and auxiliary losses give deviations from reference case.
- High power model:
  - Low scaling ratios. Moderate scaling effects, properties close to full-scale reference.
  - Expensive to build. Expensive to run. Difficult and expensive to reconfigure.
  - Safety issues. Large damage potential. Careful planning required.
- Tradeoff: 60 kVA
  - Fits existing laboratory infrastructure.

Scale: Voltage level, etc.

- Depends on power level.
- Three main ranges:
  - < 50V: Considered to be safe. Used for low power models, <1 kW.
  - < 1000V: Governed by low voltage safety regulations
  - > 1000V. Governed by high voltage safety regulations Used for high power models, > 1MW
- Standard supply voltages preferred. 230V AC ,400V AC, 690V AC.
  - 400V AC chosen. Nominal grid voltage in lab.
- Most other parameters determined by power and voltage scaling .
  - Base impedance, Inductance, Capacitance, Transformer ratio.
- Some remaining parameters:
  - Cell number, control system topology.

Series resistance



Noratel 3LT series transformers

- Difficult to scale. ESR tend to increase at low power.
- Gives additional damping of oscillations.

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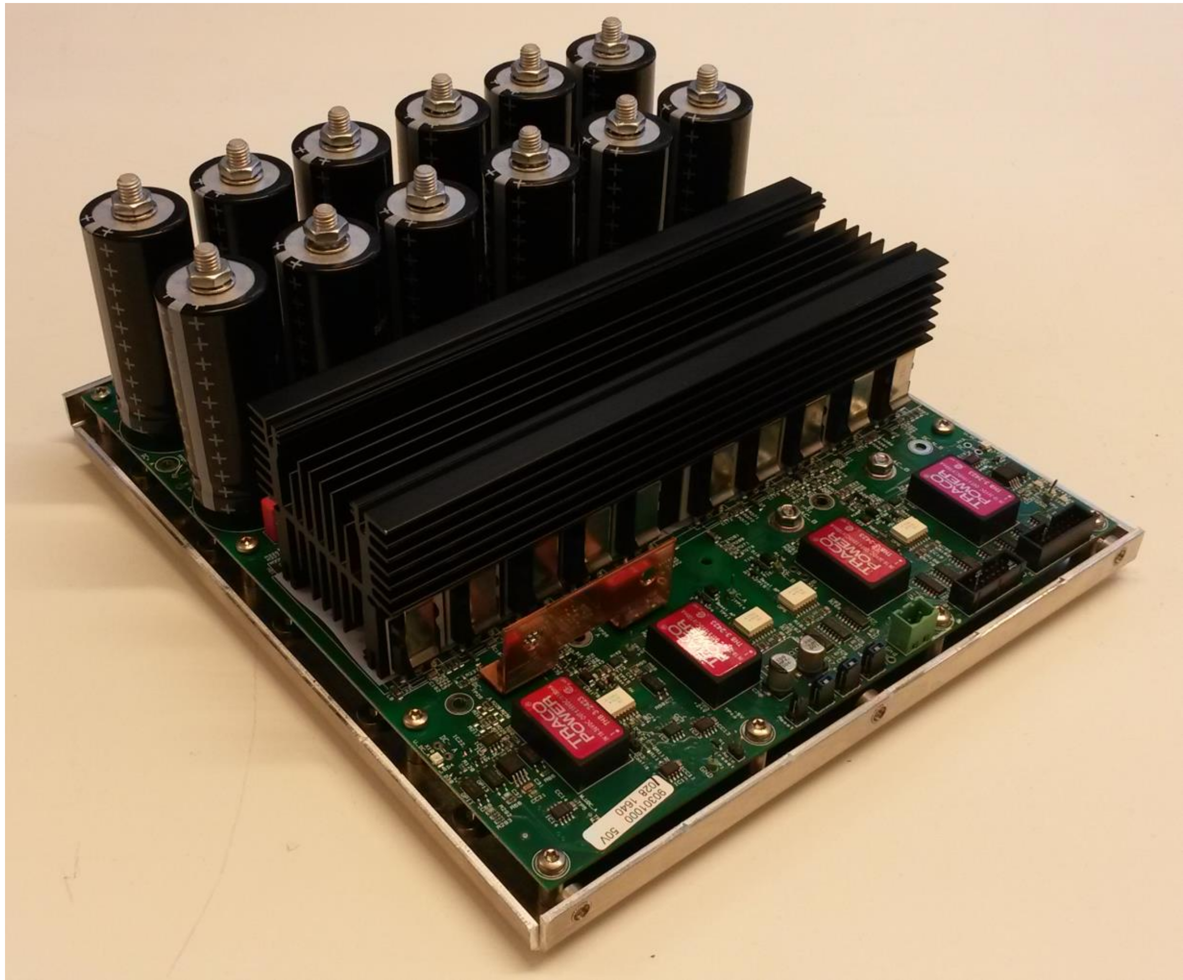
Converter specifications

	Reference	18 Halfbridge	12 Fullbridge	6 Halfbridge
Rated power	1059MVA	60 kVA	60 kVA	60 kVA
Rated DC voltage	640 kV DC	700V	700V	700V
Rated AC voltage	333 kV	400V	400V	400V
Rated AC current	1836A	85A	85A	85A
Cells per arm	400	18 Halfbridge	12 Fullbridge	6 Halfbridge
Nominal cell voltage	2 kV	50V	80V	160V
Arm inductance	50 mH	1,5 mH	1,5 mH	1,5 mH
Cell capacitance	10 mF	20 mF	15 mF	7,5 mF
Number of halfbridges	2400	108	144	36

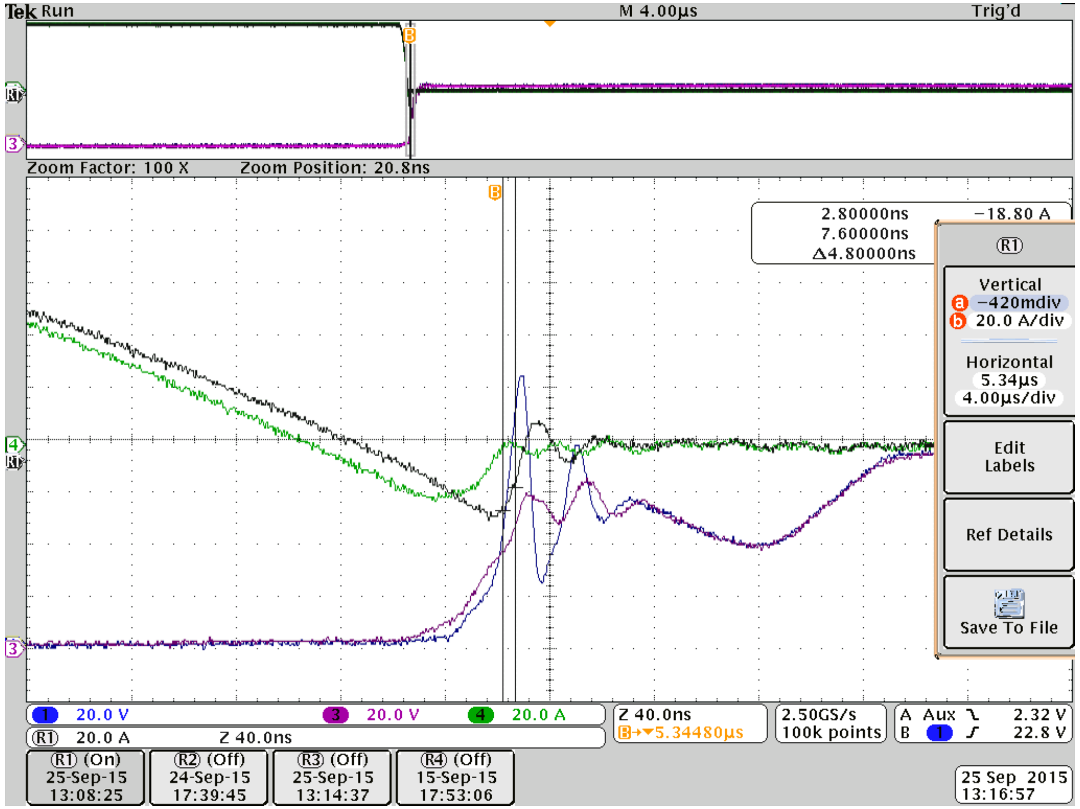
Power cell board

- Common PCB for all variants
  - 50V, 80V 160V, variants
  - Two independent halfbridges,
  - Copper rails for half or fullbridge configuration.
- Low ESR design
  - Thick copper planes in board.
  - Multiple small, low ESR electrolytic capacitors.
- Power circuit domain functions.
  - Transistor drivers, protection and interlock circuits.
  - Generic control signal interface.
  - Voltage and temperature measurements



Power transistors

- Scaled cell voltage drop: 100mV
  - MOSFETS, not IGBTs
- 5x parallel MOSFETs
  - 50 and 80V variant: 150V, 5 mOhm => ESR: 1 mOhm
  - 160V variant:: 250V , 15 mOhm => ESR 3 mOhm
  - MOSFETs types with enhanced body diodes required.
- Swiching is fast:
  - Diode reverse recovery snapoff : 20 ns.
  - Little margin for overvoltage transients.
  - Board layout extremely critical.
- Short circuit protection
  - Monitors forward conduction voltage. Trips at 0,8V => 700A



Diode turn off. 5 mm unsymmetry. Ch1,Ch3: uds, Ch4,R1: Id

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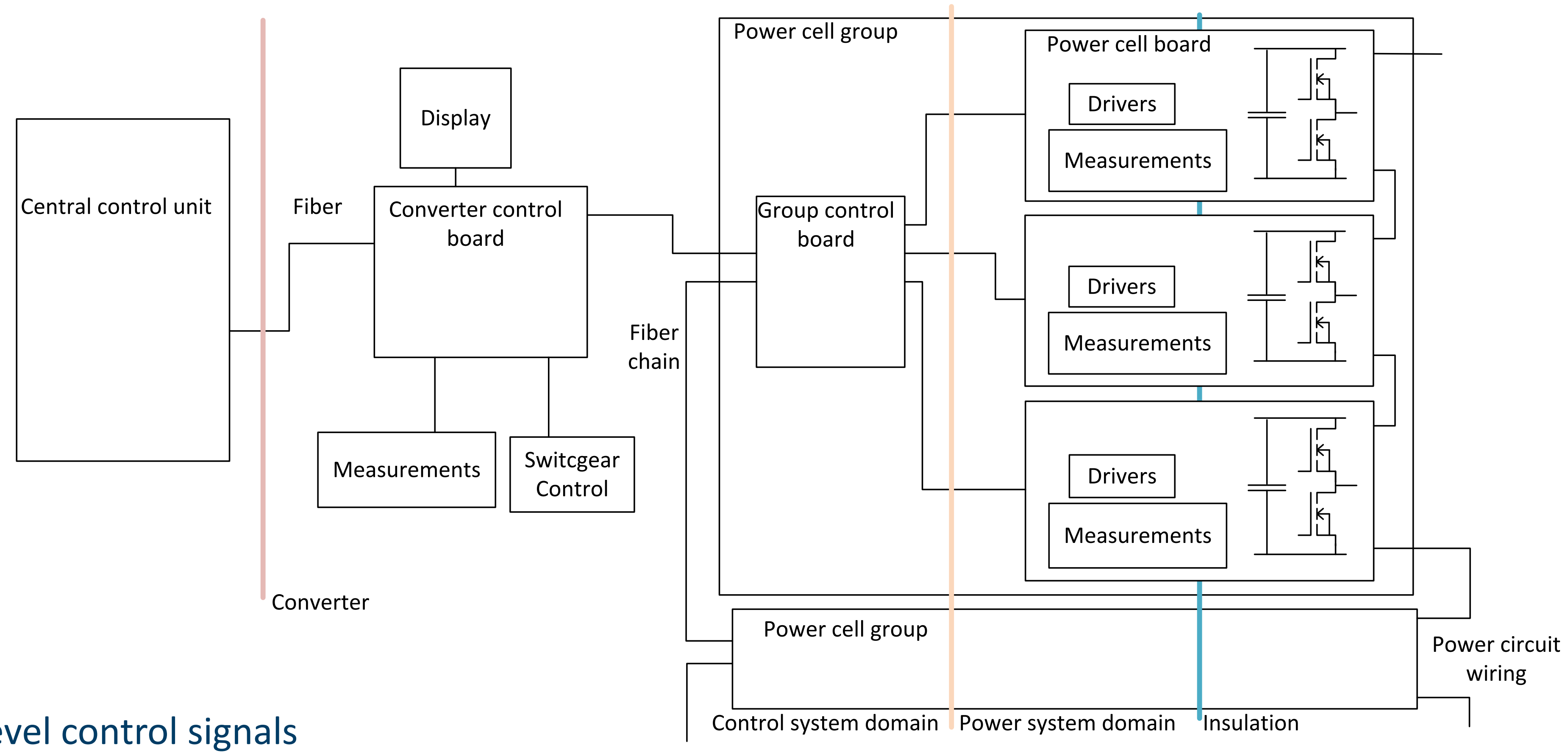
Control tasks

- Internal
  - Synchronisation of nodes.
  - Protection and state monitoring. Converter fault handling.
  - Cell voltage balancing (within an arm)
  - Arm voltage control (energy balance)
  - Circulating current control
- External
  - Phase current control
  - Active power control/DC voltage control.
  - Reactive power control/ AC voltage control
  - AC phase lock/ Frequency control/ Virtual inertia
  - Harmonic suppression, damping.
  - Grid fault handling, current limiting.

System structure

- Hierarchy:
  - Power cell board
  - Group control board.
  - Converter control board
  - Central control unit
- Optical fiber link
  - 3,75 Gbit/s
  - Chain topology
- Operation modes
  - Normal operation.
  - Development mode. Low level control signals
    - Control algorithms on external unit: OPAL-RT
    - Programming in Matlab/Simulink



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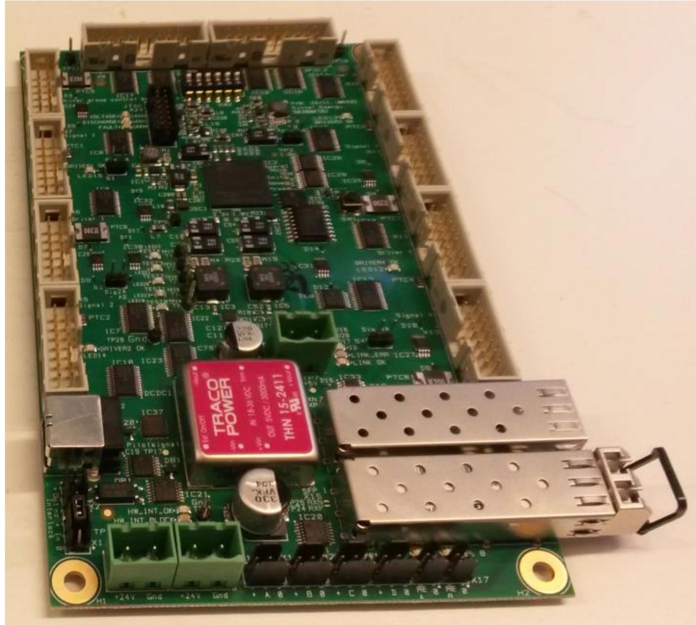
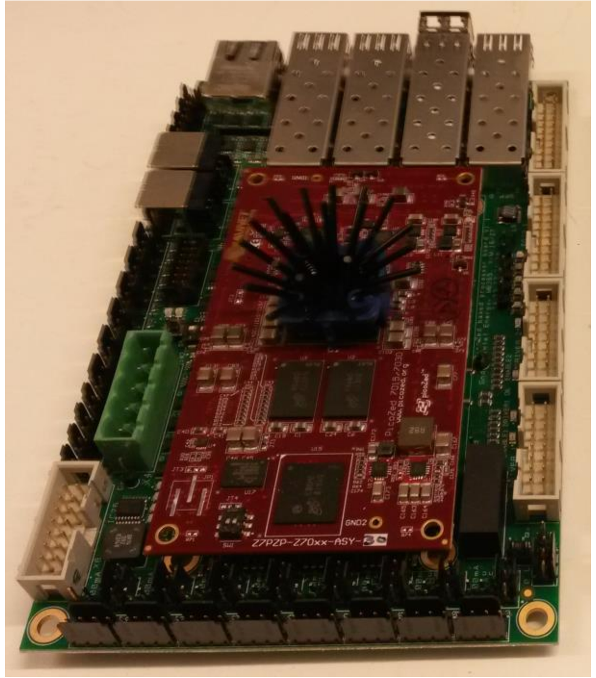
Control electronics

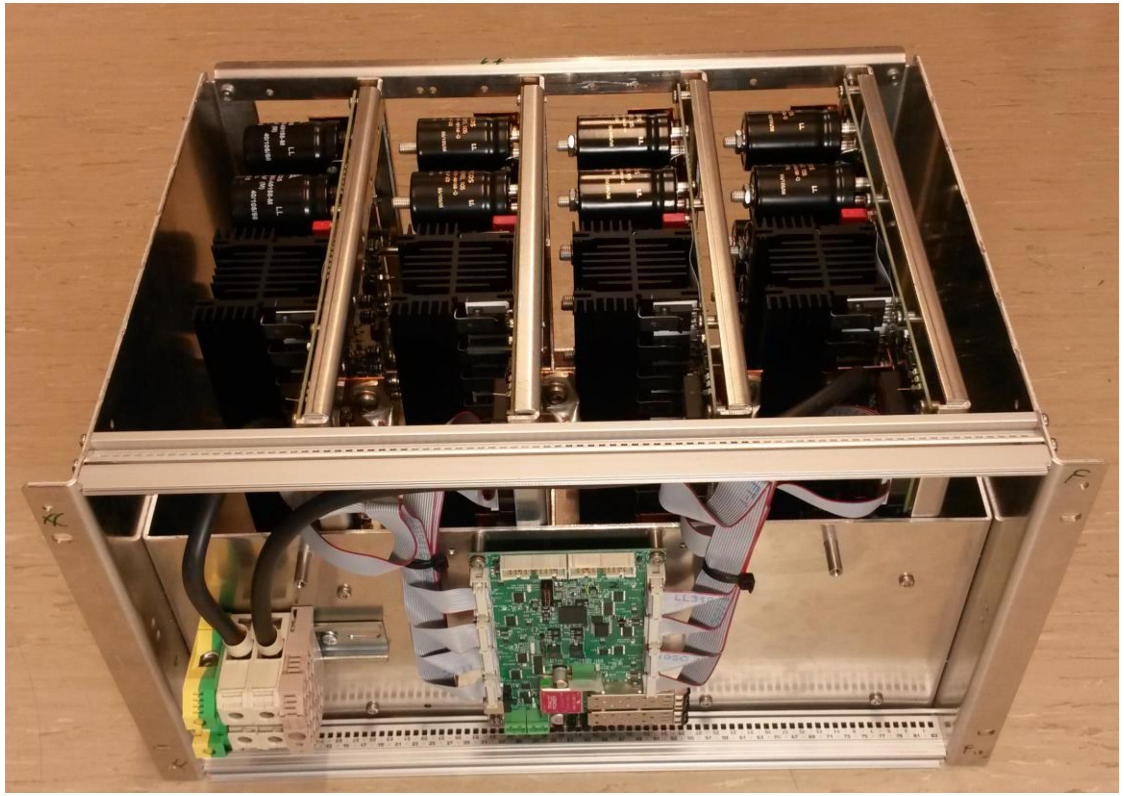
- Group control board.
  - Based on Xilinx Artix FPGA
  - Governs 3-4 power cell boards
  - Gathers measurements.
  - Distributes 24V supply to drivers.
  - Generates, distributes driver signals.
- Converter control board.
  - Designed as general purpose converter control board
  - Based on PicoZed7030 module.
  - Xilinx Zynq 7030 FPGA with ARM A9 processor.
  - 8x 40 MSPS AD converter allows oversampling.
  - Handles converter control and protection functions.





Power cell group module

- 19" subrack 6U height
  - Group control board
  - 3-4 power cell boards: 6 or 8 halfbridges, 4 fullbridges
- All connections at front.
- Power cell modules in front and back of cabinets
- Vertical boards: Convective airflow
  - No fans. Fans may be required in 6 level converter.



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19" cabinet

- 18 level halfbridge converter.
- Half filled cabinet: One phase
  - Two phases back to back.
  - Three modules per arm,
  - Two arms per phase.
- Large amount of capacitors.
  - 648 capacitor cans for 18 cell converter.

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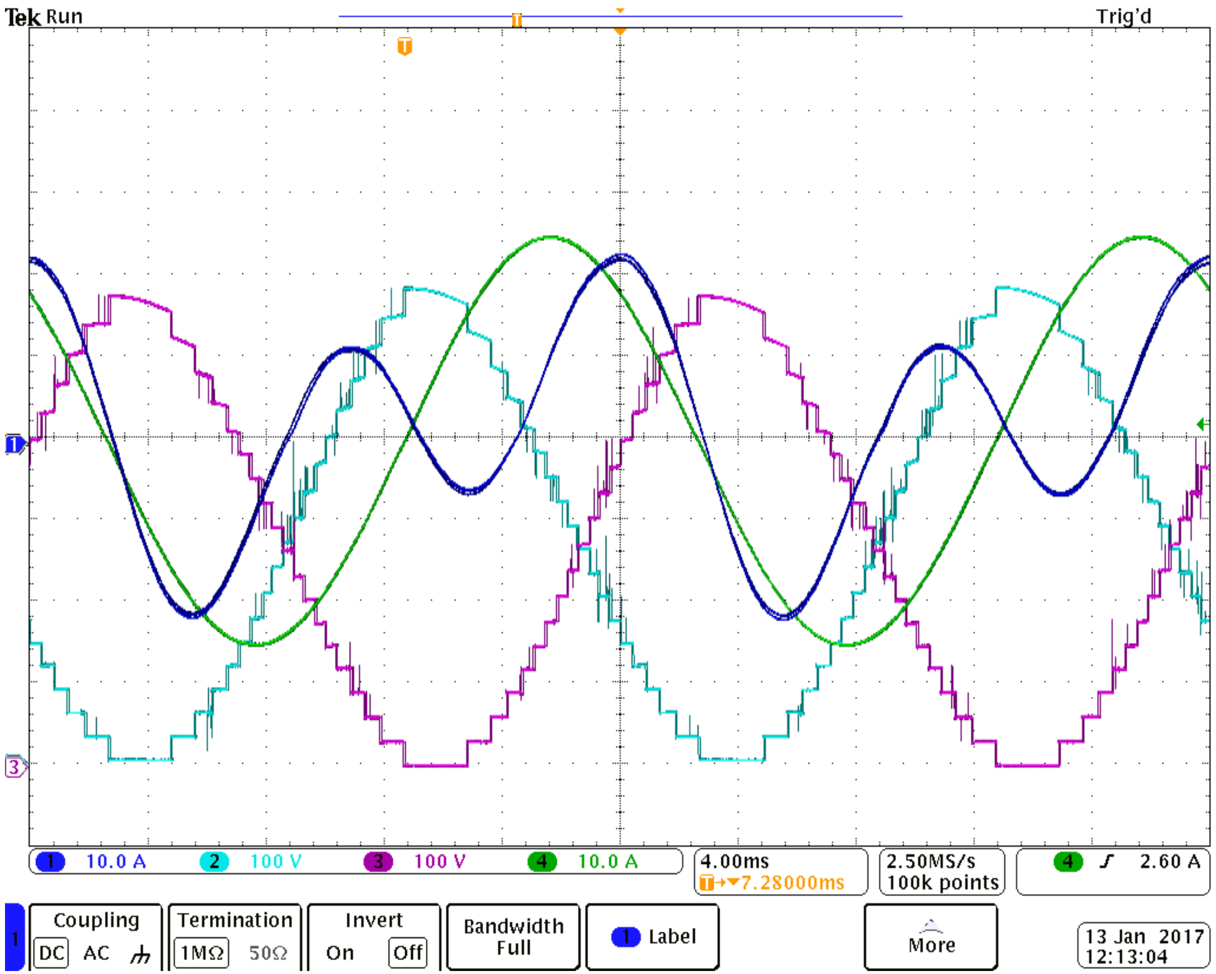
Complete 12 level fullbridge converter

- Cabinet 1:
  - Switchgear,
  - Arm inductors,
  - Control electronics,
  - Power cells phase A,B
- Cabinet 2:
  - 2: Power cells phase A,B.
- Equal layout for 18 cell halfbridge converter
- Single cabinet for 6 cell fullbridge converter

Single phase test

- Test of 18 level halfbridge converter
  - Open loop, no current control
  - Cell voltage sorting selects to be on or off
  - 100% modulation
  - Single phase RL load
  - Center tap DC capacitor bank
- Waveforms equal to simulations
  - Distorted arm current due to capacitor charging/discharging.



Ch1: Arm current, Ch2, Ch3: Arm voltages, Ch4: Phase current.

It works!

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Teknologi for et bedre samfunn