Low Power ASIC for High Temperature Applications

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Abstract: This paper describes the design and implementation of a low power/low voltage mixed signal BiCMOS ASIC that operates at temperatures up to 200℃. The ASIC is integrated into a gauge for downhole pressure and temperature measurements. It incorporates four measurement channels (CLK1-clock one, CLK2-clock two, P-pressure, T-temperature), with four high precision X-tal Pierce oscillators and a signal processing path for each channel. The output frequency from the CLK1 channel is used as a precision reference for the pressure and temperature channels and as an external clock. The ASIC is designed for high pressure transducers and incorporated into a downhole memory and wireline quartz gauge. The ASIC was fabricated into a 1.2 μm BiCMOS double poly, double metal process. The voltage supply range is from 5V to 3.3 V and the circuit occupies a silicon area of 15 mm^2. The ASIC is packaged in a ceramic 28 pins SOIC package.

I. INTRODUCTION

VLSI technologies today offer the potential for integrating mixed signal circuits as ASICs in high temperature applications. A major goal of high temperature applications is integrating analogue and digital functions toward systems on chip. This solution opens up the possibility of obtaining microelectronics circuits at a lower cost and with better reliability compared to discrete solutions. Furthermore the scale of the technology leads to reduced power supply voltages, which in turn reduces the field levels, the high temperature effects and the power consumption. As a result, low power supply voltage and high temperature operation can be used together effectively in the design of high temperature mixed signal ASICs. The market for electronics in instrumentation and control systems for downhole applications demands increased performance for gauges both in terms of duration and temperature. Many companies now require instrumentation equipment that can tolerate up to 200°C up to two months. There is no doubt as to the future market requirements - even higher temperatures for longer periods.

Process technology, physical design and circuit and layout techniques are employed to develop CMOS and BiCMOS ASICs that operate at elevated temperatures. By using a combination of these techniques, it is possible to design cost effective and reliable ASICs that can operate up to 250°C. Special circuit and layout techniques are normally used for CMOS ASICs operating near 200°C. Over this temperature and up to 250°C, the use of epi-CMOS, conservative layout rules, low power supply voltage, operating the devices into the ZTC biasing point [1][2][3] and scaling of transistor aspect ratio offer cost effective solutions for implementing reliable high temperature ASICs. Using special layout techniques significantly raises the temperature at which reliable operation is possible for mixed signal ASICs. Costs involved in these layouts derive from the additional chip area required in these methods and the extra time the designer uses to implement them. Combined with an epi-CMOS process and special circuit techniques, design rule techniques for improving high temperature performance of mixed signal ASICs is very effective.

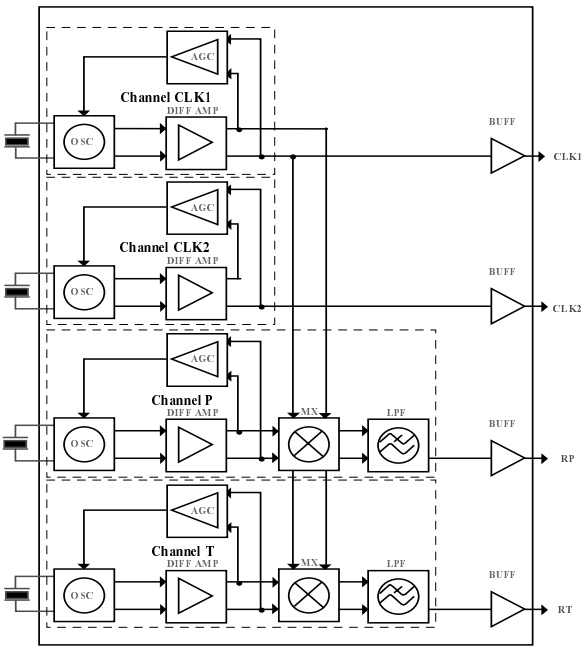

Fig. 1 ASIC Block Diagram

Furthermore, at most current high temperature applications in the range of 25-250°C, (automotive, well-logging and process industry which accounts for around 90% of the high temperature market), silicon remains the technology of choice. This is determined by the fact that the technology is the most advanced of the semiconductor technologies available and offers standard and mutually compatible processes, metallization, packaging techniques and the best overall price/performance today [4].

II. CIRCUIT DESIGN

This paper describes the design and implementation of a low voltage/low power mixed signal BiCMOS ASIC that operates at temperatures up to 200°C. The ASIC is integrated into a gauge for downhole pressure and temperature measurements.

It incorporates four measurement channels (CLK1-clock one, CLK2-clock two, P-pressure, T-temperature), with four high precision X-tal Pierce oscillators and a signal processing path for each channel. The output frequency from the CLK1 channel is used as a reference for the pressure and temperature channels and as an external clock. The block diagram of the circuit is presented in Fig. 1. The output signals can be selected by using a 2 bit channel selector. The selection of one channel will inhibit the current distribution to the channels that are not selected, thereby significantly reducing power consumption. All four channels have identical Pierce oscillators with a feedback loop that includes a differential amplifier, an Automatic Gain Control (AGC) circuit and a low power control circuit. The pressure and temperature channels have two double balanced mixer circuits that are used for generating, at the output, the difference between the reference and the pressure and temperature sensing crystals. Differential operation is maintained from the input to the output in the entire architecture in order to improve power supply rejection and accuracy.

The ASIC is owned by Geoservices S.A. and is designed for high pressure transducers and incorporated into a downhole memory and wireline quartz gauge. The ASIC was fabricated into a 1.2 µm BiCMOS double poly, double metal process. The voltage supply range is from 5V to 3.3 V and the circuit occupies a silicon area of 15 mm^2. The ASIC is packaged in a ceramic 28 pins SOIC package.

A. ASIC bias technique and power-down logic

The bias networks of the internal circuits are among the most critical components of the system design for high temperature applications. Amplifier bandwidth and gain have a strong dependence on the bias voltage/current. Furthermore, in order to minimise the problems with noise coupling and cross-talk, special consideration should be made in the design of the bias networks.

In principle one single bias network could supply all channels on the chip with the necessary bias voltages.

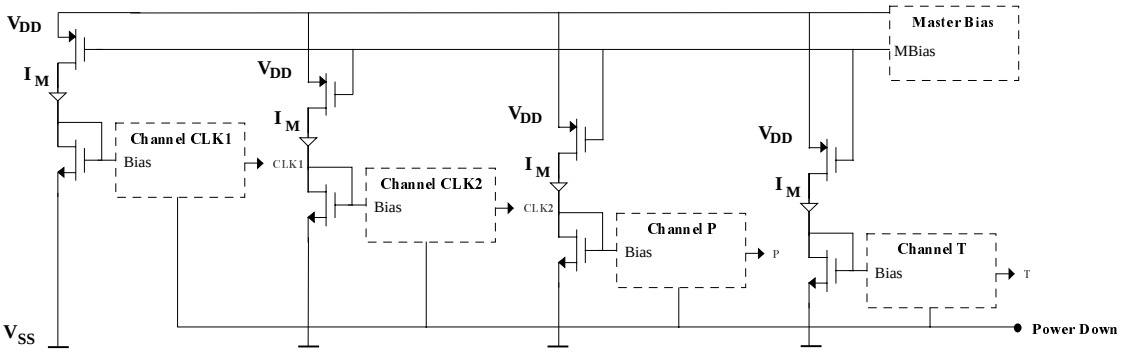

Fig. 2 Bias network for current distribution.

However, since in this application it is necessary to achieve high performance CMOS and BiCMOS analog circuits that work properly over a wide temperature range (0 to 200°C), the accurate control of the bias currents of the different blocks in the ASIC becomes an important issue. Excessive variation of bias currents with temperature and process, tends to sacrifice speed at the low extreme of bias current, and power dissipation and output voltage swing at the high end. Furthermore, the variation of bias currents with supply voltage results in poor power supply rejection (PSR) [5]. Achieving the goal of minimising the dependence of bias points on supply voltage, temperature and process variations require a bias circuit of some complexity and therefore one which is uneconomical to implement for each block of the ASIC [5]. As a result a central biasing scheme, as illustrated in Fig. 2, was chosen for the ASIC used in high temperature applications. A central master bias circuit produces a voltage which is distributed around the chip. This voltage is used by individual channel bias cells, to generate the locally required bias voltages in order to power the local circuitry.

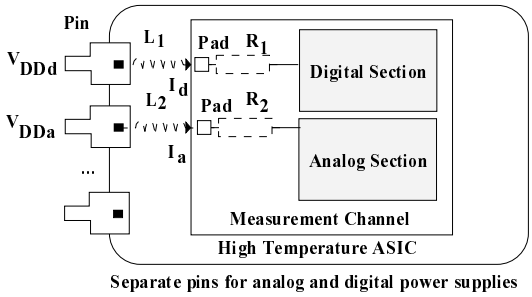

Fig. 3 Separate power pins for the low power high temperature mixed analog digital ASIC

The advantage of this technique is the flexibility of the architecture. It allows different bias cells to work at different current levels. This solution also helps in preventing crosstalk between different channels through the bias lines. Finally, by using this technique the reduction of power consumption is easily realised by implementing power down modes of operation. The master bias circuit was optimised for best temperature coefficient, absolute tolerance and power supply rejection. The circuit is designed using both bipolar and MOS transistors. In addition to the distributed bias network, the layout of the circuit uses separate power supply lines for the digital and analog sections of the ASIC as presented in Fig. 3. This complete separation in the biasing of the two sections gives obvious advantages in terms of noise limitation, even if special care must be paid to substrate biasing.

B. Oscillator Design Considerations

The oscillator of each channel was implemented using Pierce type architectures which offer a relatively low power consumption, high frequency stability and good signal form for frequencies above 3 MHz. Furthermore, the Pierce oscillator has the ability to operate properly when the circuit stray capacitance and inductance are large and is relatively simple to design [6][7].

The stability in operation is assured by using an automatic gain control (AGC) circuit. The AGC block MOS transistors operating in strong inversion saturation and requires an external capacitor and resistor [9]. This adds to the number of the components necessary to implement the downhole instrumentation system but improves the flexibility of the circuit. At start-up the AGC delivers the extra current required by the oscillator in order to reduce the start-up time. Furthermore, when stable conditions are reached, the AGC regulates the oscillator power consumption to ensure a proper and stable operation. By doing this, the power consumption is kept at minimum. The transient analysis of the oscillator requires an extensive simulation time due to the large Q-value of the crystal. The start-up simulation was performed in 1 week on a HP J200 computer.

C. Differential Amplifier

The differential amplifier circuit is presented in Fig. 4. The differential gain of the circuit is provided by the first differential pair stage and the push pull output stage, which together provides a reasonable amount of gain. The gain of the circuit is 30 dB at 25°C.

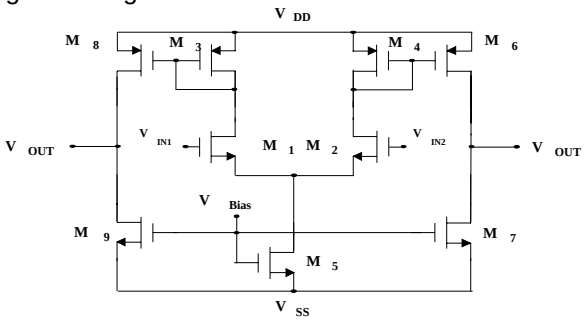

Fig. 4 Differential Amplifier

The circuit provides a fair output current and maintains a low power consumption with a capacitive load of 10 pF. The gain of the amplifier varies insignificantly (2 dB) with temperature (25 to 200°C) at frequencies below 10 MHz.

A number of specific layout techniques are applied for current leakage reduction and latch-up for high temperature operation. For the reduction of the

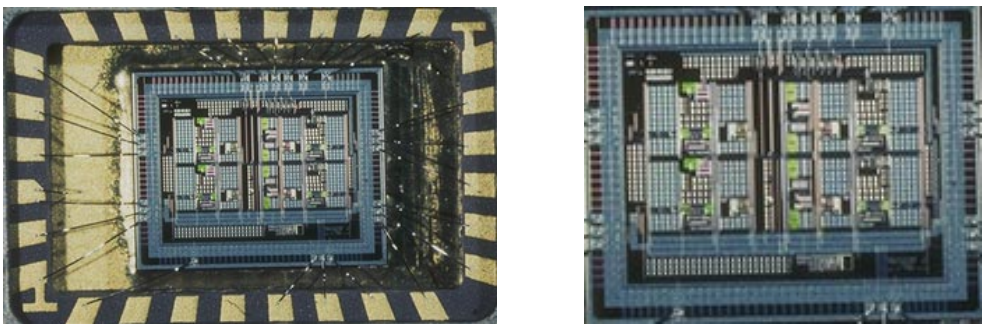

Fig. 5 Microphotograph of the 1.2 µm BiCMOS low power high temperature ASIC

described in [8] was used for design. The AGC uses

leakage currents a number of techniques were applied [4][10]:

- Guarding
- Special device layout (common centroid and interdigitized structures)

Physical layout adjustments were employed to compensate for the loss of surface mobility which comes with high temperature. The ASIC microphotograph is shown in Fig. 5. The ASIC occupies an area of 15 mm^2 and is encapsulated into a 28 pin SOIC package.

III. MEASUREMENT THEORY

The sensors used together with the high temperature ASIC have a typical frequency range between 15 kHz at room pressure and 60 kHz at full pressure for the pressure sensor and between 10 kHz at 180 °C and 60 kHz at 25 °C for the temperature sensor.

TABLE I

FREQUENCY SENSITIVITY- PRESSURE SENSOR

Pressure sensor	Sensitivity
34 483 kPa	0.655 Hz/Pa
68 966 kPa	0.437 Hz/Pa
110 345 kPa	0.306 Hz/Pa
139 310 kPa	0.290 Hz/Pa

TABLE II

FREQUENCY SENSITIVITY -TEMPERATURE SENSOR

Temperature sensor	Sensitivity
25°C	135 Hz/°C
180°C	260 Hz/°C

Typical frequency sensitivities of the output signals for pressure and temperature sensors are presented in Table I and II [10].

The change in the frequencies of the output signals of a typical temperature and a typical pressure transducer with changes in temperature and pressure are presented in Fig. 6.

The nominal change in frequency of the temperature sensor over the 25 to 175°C range is shown in Fig. 6a.

The change in frequency of the pressure sensor with changes in pressure and temperature (25 and 175°C) is presented in Fig. 6b.

A. Frequency Counting

The pressure resolution that is available from a downhole transducer system is a function of the user's time base frequency, the gate time during which the frequency is counted, the pressure sensitivity of the pressure sensor and the method of frequency counting. There are mainly two methods of frequency counting used in this type of applications: direct frequency counting and period counting. Direct frequency counting is simple and can be used with any timebase. It is the preferred method if the user's timebase frequency is lower than the pressure sensor frequency (15-70 kHz). Direct frequency counting uses the timebase frequency to determine the gatetime during which the sensor frequency is counted. Usually, the implementation provides for the gatetime, t, to be determined by a fixed number of counts of the reference timebase frequency [11]. Period counting, also called reciprocal counting, uses the sensor frequency to determine the gatetime during which the reference timebase frequency is counted. This method can provide higher resolution than direct frequency counting using a high frequency timebase. The user's signal processing system determines the sensor frequency from the reference frequency and the number of counts of the sensor and of the reference during the gatetime [11].

IV. RESULTS

The circuits were tested with respect to temperature range, leakage current and frequency stability. The silicon circuit was mounted in a ceramic SOIC 28 package and the cavity was sealed and filled

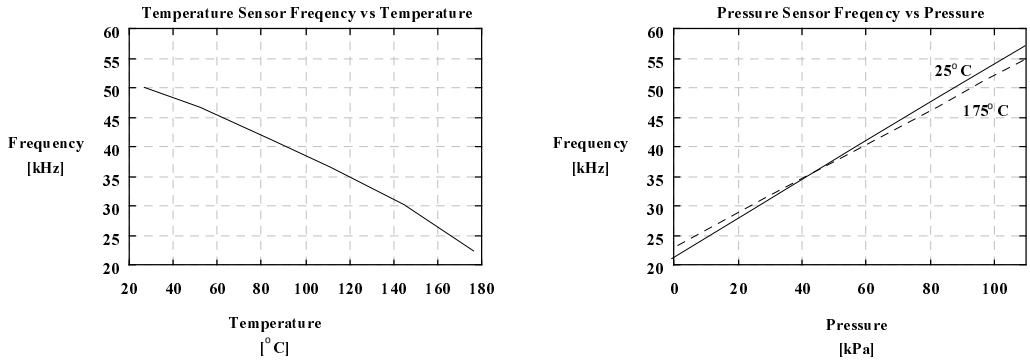

Fig. 6 Frequency change of temperature and pressure signal over temperature and pressure

with nitrogen. The tests were carried out both at the wafer level and in CSOIC package.

The test set-up has employed a PCB specially designed for high temperature applications and the upper operating temperature was specified as 200°C.

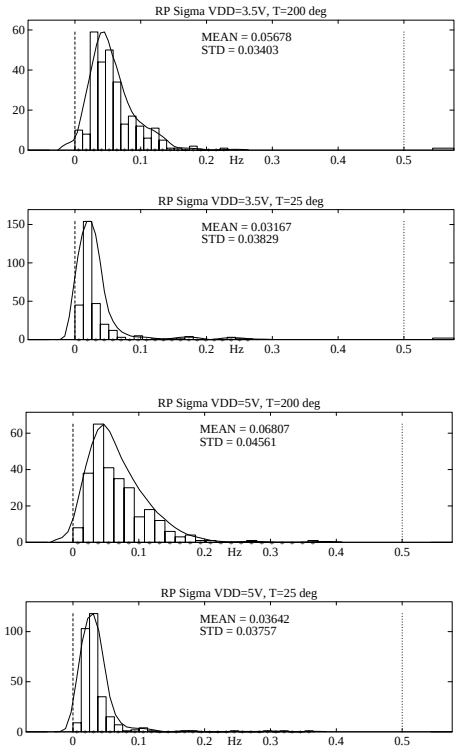

Fig. 7 Typical values for Sigmas measured for the pressure channel at wafer sort

The test results are presented in Fig. 7 for the pressure channel at 5V and 3.5V voltage supply and 25 and 200°C. Similar results were obtained for the temperature channel. As seen from Fig. 7 the frequency at the output of the ASIC is very stable over the whole temperature range. The power consumption of the circuit varies from maximum 20 mW for 5V operation at 200°C with all the channels activated down to 8 mW for 5V operation at 25°C with only one channel activated. The power consumption for the lower voltage operation is scaled down accordingly.

V. CONCLUSION

A low power/low voltage ASIC dedicated for high temperature applications up to 200°C has been developed and tested. The circuit was designed for use with high pressure/high temperature transducers and was incorporated into a downhole memory and wireline quartz gauge. The ASIC was fabricated into a 1.2 µm BiCMOS double poly, double metal process. The voltage supply range is from 5V to 3.3 V and the circuit occupies a silicon area of 15 mm^2. The circuit integrates a controlled biasing network that permits the power down of the different modules that are not in use, considerably reducing the power consumption. The ASIC is packaged in a ceramic 28 pins SOIC package.

VI. REFERENCES

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