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TECHNICAL PAPER

3D System-on-Chip technologies for More than Moore systems

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Abstract 3D integration is a key solution to the predicted performance problems of future ICs as well as it offers extreme miniaturization and cost-effective fabrication of More than Moore products. Through silicon via (TSV) technologies enable high interconnect performance compared to 3D packaging. At present TSVs are associated with a relatively high fabrication cost, but research world wide strive to bring the cost down to an acceptable level. An example of a 3D System-on-Chip (3D-SOC) technology is to introduce a post backend-of-line TSV process as an optimized technology for heterogeneous system integration. The introduced ICV-SLID process, that combines both TSVs and bonding, enables 3D integration of fabricated devices. Reliability issues related to thermo-mechanical stress caused by the TSV formation and the bonding are considered. 3D-SOC technology choices made to realize a heterogeneous ultra-small IC stack for a wireless tire pressure monitoring system (TPMS) as an automotive application are described.

1 Introduction

Performance and productivity of microelectronics has been increased continuously over more then four decades due to the enormous advances in lithography and device technology. However, today it has become questionable if this so-called "More Moore" development alone will be able to overcome the predicted performance and cost problems of future IC fabrication. Moore's law will encounter the "red brick wall" somewhere in the 32–22 nm nodes. On one hand there are simply cost concerns e.g. related to extreme UV lithography. On the other hand, one of the fundamental issues of advanced devices is RC delay caused by the on-chip wiring. The latter obstacle is a major challenge for future IC fabrication and demands the implementation of ultra low-k dielectrics for multilevel metallization. Unfortunately, the introduction of applicable technologies was delayed several times and SEMATECH stated in 2008: "Materials selection to the RC problem are drawing to close" (Arkalgud 2008).

The ITRS roadmap (ITRS 2007) predicts 3D integration as a key technique to overcome this so-called "wiring crisis". The corresponding solution will most probably be based on through silicon via (TSV) technology. But which microelectronic products based on TSV technologies are at present actually in the market? Figure 1 shows a roadmap for applications of 3D integration. CMOS image sensors using a "via last" approach (thinning of silicon before TSV formation) with via diameters of about 50 μm and similar silicon thicknesses have been already introduced in the market mainly driven by form factor. 3D stacking of DRAM memories by applying TSV technology is in development and will be introduced soon (year 2010). Subsequently the stacking of Flash memories is expected to be introduced. The evolution of the corresponding fabrication technologies will result in combined DRAM/Flash products with TSV diameters of <5 μm in ultrathin silicon of less than 20 μm thickness. Chip-on-Chip (CoC) stacking of memory and logic devices without TSVs is already widely introduced in the market. Applying TSV technology

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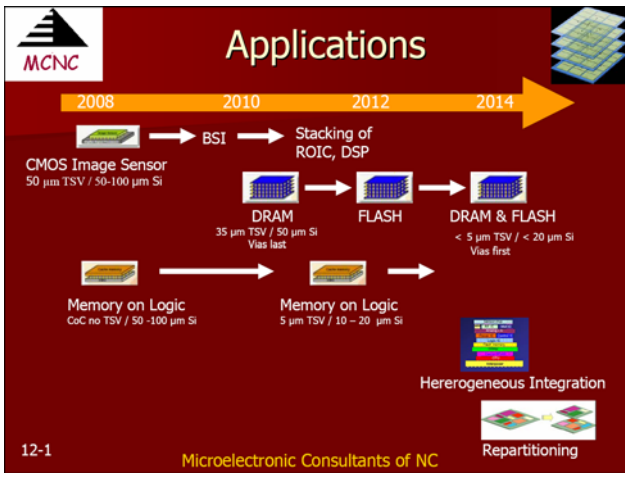

Fig. 1 Roadmap of applications based on 3D integration (courtesy of Phil Garrou, MCNC)

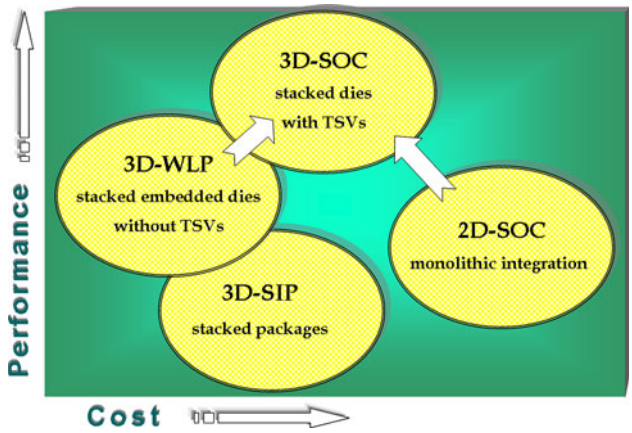

Fig. 2 Qualitative comparison of different system integration technologies

for memory on logic will increase the performance of these advanced products and simultaneously shrink their form factor.

In addition to the enabling of further improvement of transistor integration densities ("More Moore"), 3D integration is a well-accepted approach for so-called "More than Moore" applications. Wireless sensor networks (e.g. e-CUBES® 2009) represent a typical example for such heterogeneous systems with the need for smart system integration of ICs, passive components and MEMS.

2 Definitions and motivations

3D integration is generally defined as fabrication of stacked and vertically interconnected device layers. The large spectrum of 3D integration technologies can be reasonably classified within three categories:

1. Stacking of packages (or substrates)
2. Die stacking (without TSVs)
3. TSV technology

According to the "Handbook of 3D Integration" the first two categories can be catalogued under "3D Packaging". The third category can be further separated into "via first" and "via last" TSV technologies. Taking into account that there are different definitions for "via first" and "via last" we prefer to use the terms "TSV prior stacking devices" and "TSV post stacking devices" (Garrou et al. 2008). What are the criteria for a technology choice? Cost will be always a main criterion for 3D integrated products (see Fig. 2). Besides form factor improvement, the key driver for TSV based 3D-SOC technology can however not be low cost fabrication [estimated >400 US$ per wafer, I-micronews (Yole Developpement) 2008] but rather the obtainable high performance enhancement compared to 3D packaging (3D SIP). This said TSV technology has the potential to be less costly than today's state-of-the-art for mixed technologies products, monolithically integrated Systems-on-a-Chip (2D-SOC).

3 Technologies

In more than two decades, great research efforts were made in the area of 3D integration, starting in the 1980s by e.g. IBM, NEC, Siemens and Fraunhofer. Since the early 90's Fraunhofer Munich has worked on stacking technologies using vertical inter-chip vias—ICVs (today's common term: through silicon vias—TSVs), focusing on 3D integration concepts which take advantage of wafer level processing to achieve the highest miniaturization degree, excellent electrical performance and enable high volume cost-effective fabrication (Ramm et al. 2008a).

A "via first" post backend-of-line 3D integration technology (see Fig. 3) based on TSVs and stacking of devices by intermetallic compound bonding (ICV-SLID) has been developed and evaluated (Ramm et al. 2008b). The enabling processes show up as especially sophisticated when studying the production requests (e.g. TSV formation on fully processes IC devices with complex BEOL layer structures). Several characteristic features of deep reactive ion etching, deposition of dielectrics and metallization might result in reliability problems of high aspect ratio TSVs. In consequence processes optimized specifically for TSV technologies have to be applied.

More than Moore products are typically fabricated by chip-to-wafer stacking of non-identical devices. The basic conditions for the application of intermetallic compound bonding have to be considered carefully. Two critical

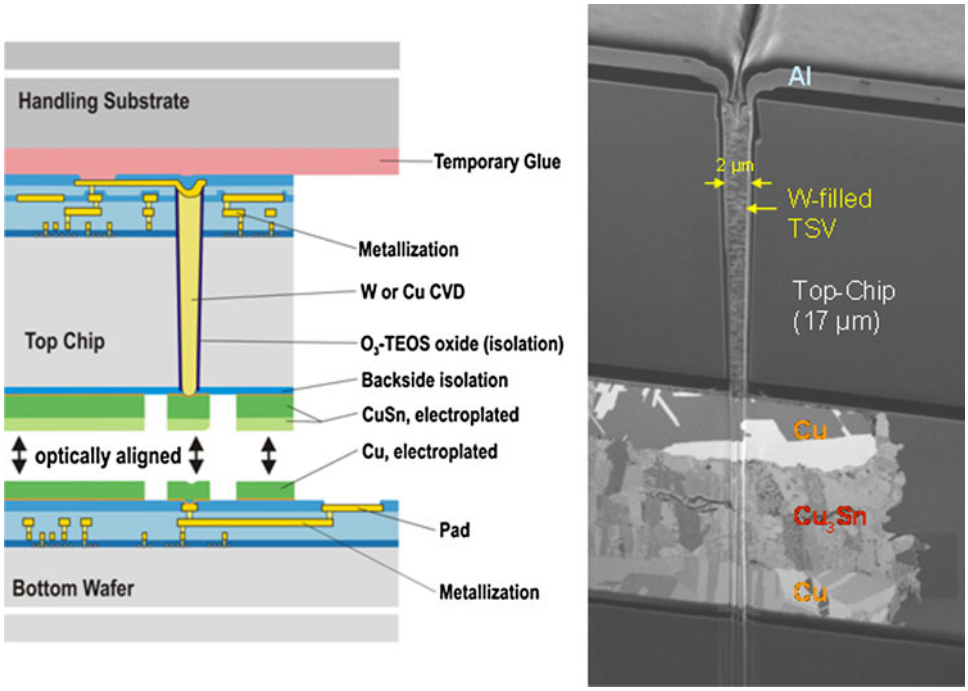

Fig. 3 ICV-SLID technology—a "TSV prior stacking" post BEOLprocess. *Left* Schematic for aligned stacking of the thinned and stabilized top chip (with completely processed TSVs) to the bottom device wafer. *Right* FIB of a 3D integrated device stack, showing a cross section with CVD-W filled TSVs and the Cu_3Sn intermetallic compound bond layer which provides both the electrical and mechanical interconnect

topics are the topography of the devices to be stacked and the possibility of getting high mechanical stress built into the final 3D-IC stacks due to the TSV formation and/or the bonding process. Corresponding process optimization is required to overcome these possibly limiting conditions. A qualification process for the introduction of such new technologies into fabrication has to be accompanied by reliability evaluations, e.g. thermo-mechanical simulations taking into account the successive evolution of mechanical stress during processing (Ramm et al. 2008a, b). The locations of highest loading during processing and operation (simulated by thermal cycling) have been identified by monitoring stress and plastic strain building up due to thermal mismatch. It can e.g. be shown that in the case of W-filled TSVs, the maximum stresses and strains are observed not in the bulk region of the TSV but in the upper part of the via between IC metal layer and the tungsten filler. However, if the tungsten is replaced by a copper-filler, more stress is induced in the TSV itself. As a consequence, process steps are adjusted to minimize stress and thereby assure higher reliability. Besides the TSV formation, the wafer bonding process can build high mechanical stress into a 3D-IC stack—particularly for More than Moore systems. In general ready-processed and thinned devices with different backend-of-line compositions (metals/dielectrics compound on thin silicon) have to be stacked for such systems. Variations in lateral die dimensions will be "freezed" at the specific bonding temperature as a result of different thermal expansions. The bonding temperature (e.g. up to 400°C for Cu–Cu bonding) can be far above room temperature and lead to large mechanical stresses in the chip stack, but this will depend on choice of bonding technology.

At present there does not exist one unique 3D integration technology which is suitable for the fabrication of the complete variety of suggested 3D integrated systems. On the contrary, even one single More than Moore product may need several different 3D integration technologies for a cost-effective fabrication. Wireless sensor systems represent an excellent example for the need of a suitable mixture of technologies. Consisting of MEMS, application specific ICs, memories, antennas and power modules they can only be fabricated in a cost-efficient way by application of specifically optimized 3D technologies to integrate the different sub-modules. Within the European Integrated Project e-CUBES a variety of 3D integration technologies was developed for the application of extremely miniaturized wireless sensor nodes. Figure 4 shows schematics of the main 3D integration concepts for the realization of the application demonstrators (processes and characteristics are described in http://www.ecubes.org).

The enabling technologies are optimized for the 3D integration of the application layer, consisting of a processing unit and a sensor function. The sensor node which was selected for the demonstration of a 3D integration concept for an automotive application is a tire pressure monitoring system (Schjølberg-Henriksen et al. 2009). The 3D integrated key element of the monitoring system

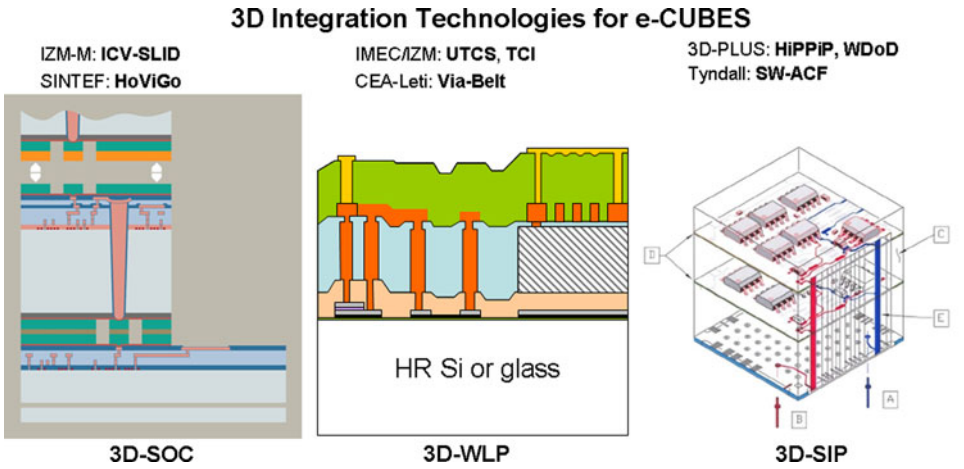

Fig. 4 3D integration concepts for the fabrication of e-CUBES® application demonstrators (miniaturized wireless sensor nodes)

is a stack of four silicon devices. The stack includes a microcontroller, an RF transceiver and a pressure sensor as shown in Fig. 5. The transceiver die and the cap of the sensor die were processed with TSVs and matching routing and interconnection layers on relevant sides. The ICV-SLID technology was optimized for the fabrication of e-CUBES processing units (3D-ICs). For the 3D MEMS stacking a new cost-effective 3D-SOC process was developed: Hollow-Via Gold Stud Bump Bonding—HoViGo (see http://www.ecubes.org). A cost-effective interconnection technique combining Au stud bump bonding and glass wafers with silicon vias was applied and evaluated to stack the sensor and BAR to the 3D-ICs Optimized processes of these 3D-SOC technologies were successfully used in the development of the 3D-IC/MEMS stack of a TPMS wireless sensor node (see Fig. 5).

4 Conclusions

3D integration represents not only an enabling technology for further improvement of transistor integration densities ("More Moore"), but in addition a well-accepted approach for so-called "More than Moore" applications. Wireless sensor networks (e.g. e-CUBES®) represent a typical example for such heterogeneous systems with the need for smart system integration of ICs and MEMS. The application of 3D integration for the production of MEMS/IC systems has been reported in this paper. Emerging 3D integration technologies were optimized and applied for the fabrication of tire pressure monitor system (TPMS) sensor nodes. The fabrication processes for the 3D integration of ICs using through silicon vias (TSV) enable high performance interconnections but show up as more sophisticated

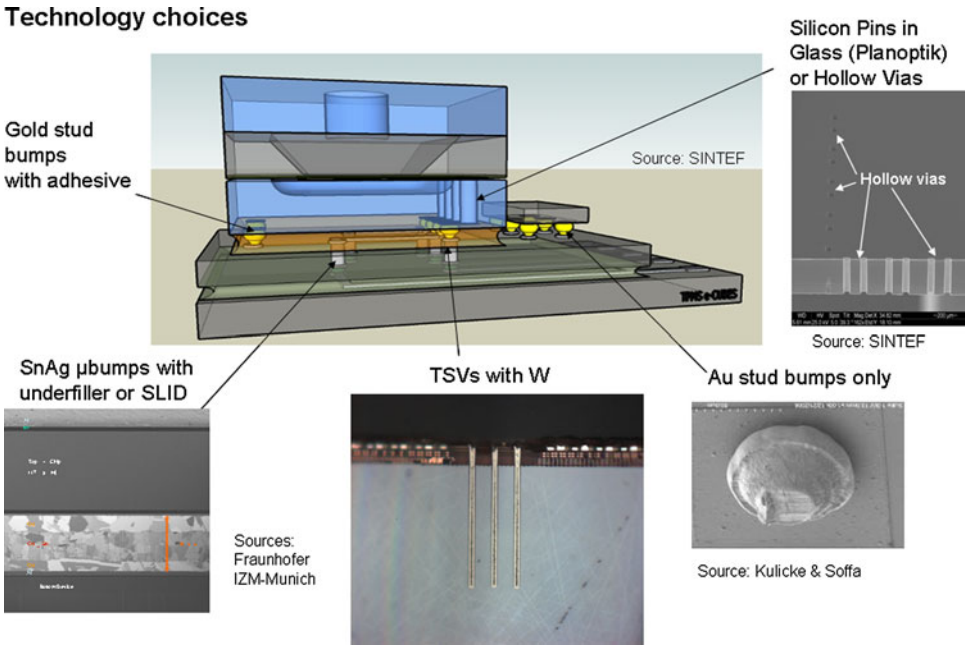

Fig. 5 Enabling technologies for the e-CUBES® automotive application demonstrator—3D-IC/MEMS stack of a TPMS wireless sensor node

and in consequence more costly when looking into production requests. Cost is certainly a key driver for 3D integrated products but the cost issue must be a long term consideration for advanced More than Moore systems rather a long term one (highly dependent on application and markets). Performance improvements and increased density of functionality are the short term drivers. However, manufacturability and reliability of 3D fabrication processes are the basic requirements that must be considered early when determining the choice of the technologies for future products. Although there are significant challenges regarding the introduction of 3D-SOC integration technologies to production lines, no real "show stopper" has been identified.

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