

MoSiS

Eureka Σ1 3674 Programme, ITEA2 project ip06035  
SINTEF / Andreas Svendsen, 2009-01-15

# TCL: Train Signaling with Automatic Code Generation

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INFORMATION TECHNOLOGY FOR EUROPEAN ADVANCEMENT

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## Overview

- Railway Interlocking System
- Current Development Process
- Train Control Language (TCL)
- Safety Issues
- Variability Modeling
- Conclusion

SINTEF ABB 2

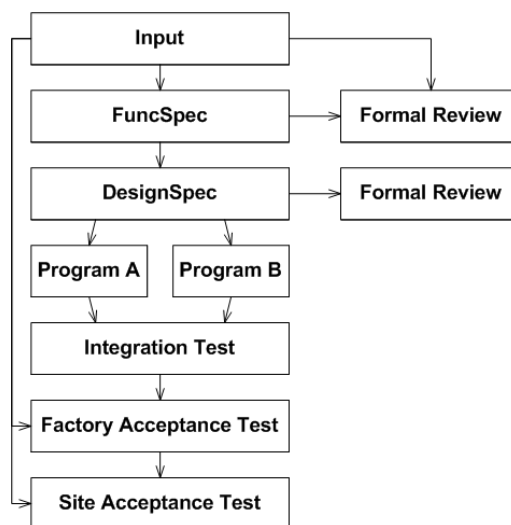
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## Railway Interlocking System

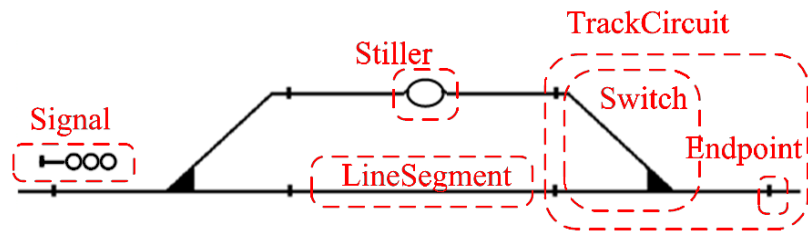
- Prevent conflicting and dangerous train movements
- Computer based interlocking (CBI)
  - Source code created for every station
- Based on Programmable Logic Controller (PLC)
- Two PLCs with diversified code to enhance safety



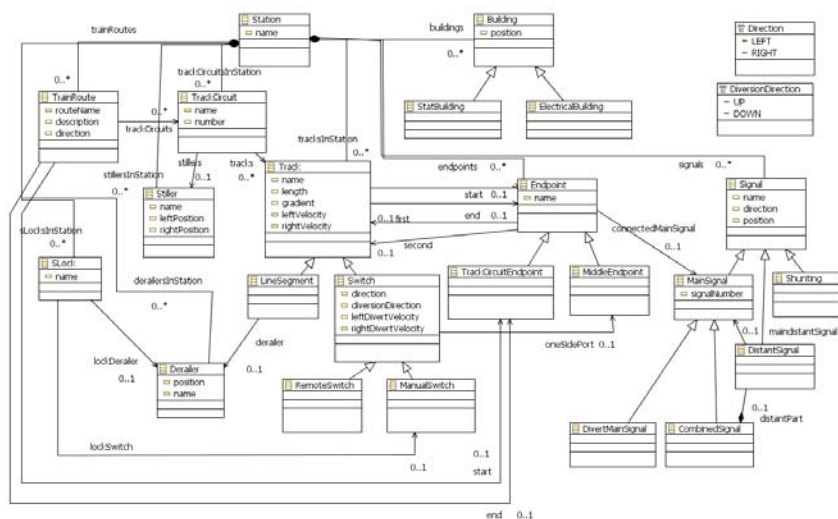
## Current Development Process



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## TCL – Graphical Editor

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## TCL – Tools

```
Str_br_1(Hj_Str_br:=Felles.Hj_Str_br,
Sf_n1_F := Sf_A.Fk,
Sf_n2_F := Sf_B.Fk,
TP := TID.tStr_br,
Str_br => Felles.Str_br);
```

| Train Route Description  | Train Route | Stiller B |   | Stiller A |   | Stiller II |   | Stiller I |   | Switch V2 | Switch V1 | Train Routes |   |     |     |    |    |    | Track Circuits |     |     |   |   |    |    |   |   |
|--------------------------|-------------|-----------|---|-----------|---|------------|---|-----------|---|-----------|-----------|--------------|---|-----|-----|----|----|----|----------------|-----|-----|---|---|----|----|---|---|
|                          |             | L         | N | B         | A | M          | O | A         | N |           |           | B            | M | B12 | B11 | L2 | N1 | M2 | O1             | A12 | A11 | L | B | O1 | O2 | A | M |
| From StationA to Track 1 | B12         | -         |   |           |   |            |   | -         | + |           |           | -            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + | + |
| From StationA to Track 2 | B11         | -         |   |           |   |            |   |           |   |           |           | +            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + |   |
| From Track 1 to StationA | L2          |           |   |           |   |            |   |           | + |           |           | +            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + |   |
| From Track 2 to StationA | N1          |           |   |           |   |            |   |           |   |           |           | +            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + |   |
| From Track 1 to StationC | M2          |           |   |           |   |            |   |           |   |           |           | +            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + |   |
| From Track 2 to StationC | O1          |           |   |           |   |            |   |           |   |           |           | -            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + |   |
| From StationC to Track 1 | A12         |           |   |           |   |            |   |           |   |           |           | +            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + |   |
| From StationC to Track 2 | A11         |           |   |           |   |            |   |           |   |           |           | -            | + | +   | +   | +  | +  | +  | +              | +   | +   | + | + | +  | +  | + |   |

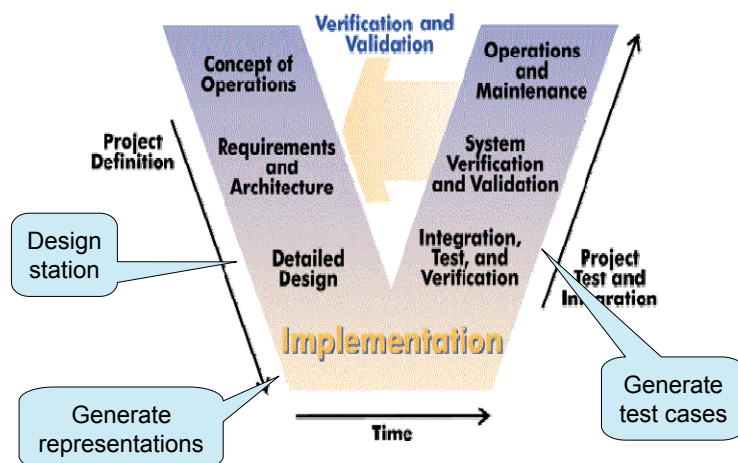
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## Ensuring Completeness and Consistency

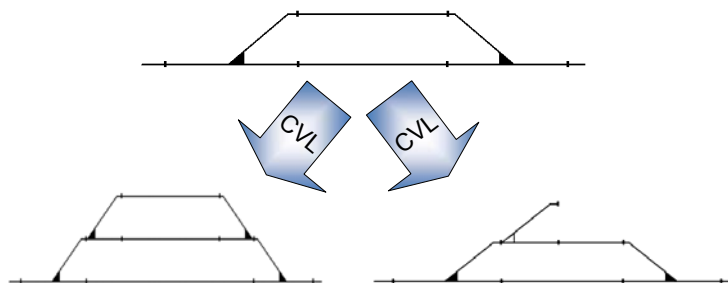
- **Representations generated from a common model**
  - Consistency between the representations can be guaranteed
- **Constraints on the editor guarantees completeness**
  - By not omitting any necessary elements
- **Still need to validate and test the results**
  - To ensure a completely safe system



## TCL - Safety Integration

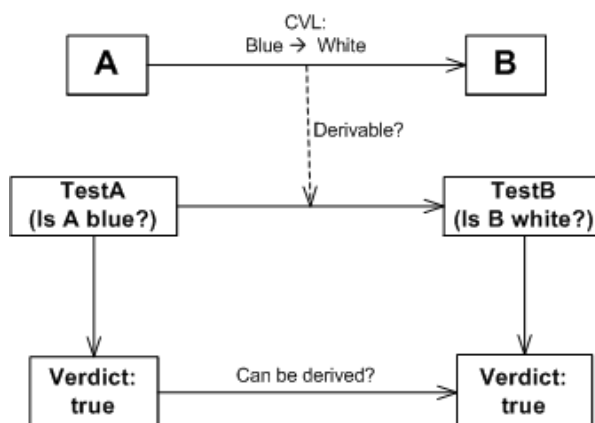


## Variability Modeling



Can it be proven that these new stations are correct and safe?

## Variability Modeling (2)



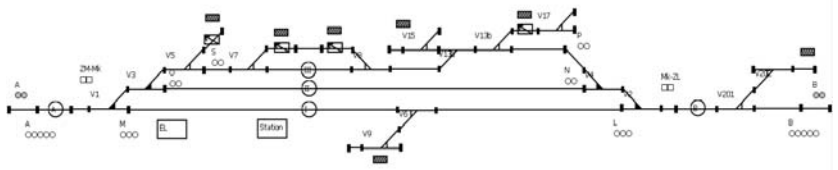


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## Station M

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|     |     |      |    |     |      |    |     |      |     |     |      |
|-----|-----|------|----|-----|------|----|-----|------|-----|-----|------|
| AS2 | AS1 | AS11 | M2 | OS1 | SS11 | L2 | N01 | P011 | OS2 | OS1 | OS11 |
| M   | A   | S    | OS | OS  | OS   | Z  | B   | L    | N   | OS  |      |







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## Conclusion

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- **A DSL can improve the development process of interlocking systems**
- **Representations directly generated from the graphical model:**
  - Interlocking table, source code, tests, etc.
- **Assures consistency and completeness**
- **Comprehensive validation of the code generators is needed**
- **The approach has definite potentials**





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