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D 5.4
Final CSD PZT cluster coater tool: Application note

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PU	Public	x
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential , only for members of the consortium (including the Commission Services)	

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Deliverable name:	Final CSD PZT Cluster coater tool: Application note
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Abstract

The Solar-Semi CSD (coating spin deposition) tool MC204 CSD was originally developed for resist coating applications in the semiconductor and MEMS industry. This tool has proven its industrial reliability with more than 50 installations. It consists of a basic platform with a central robot for wafer handling, a carrier loading unit, the coater system, a hotplate stack, including a cool plate and a transfer station to an RTP (Rapid Thermal Processing) furnace. Furthermore a second transfer robot permits to move wafers to the RTP oven, dogged onto the basic platform.

The CSD tool is able to create highly uniform crystalline PZT layers on 6” and 8” wafers with the ability of a continuous wafer edge handling to feature wafer front and backside coating.

In a typical process sequence wafers will be moved to the coating system to obtain a PZT layer by spinning on a liquid precursor and is then transferred to the hotplate for pyrolysis. This sequence of spin on, hotplate pyrolysis will be performed 4 times to obtain a layer thickness of typically 400 nm, followed by a RTP step for layer crystallization. In order to obtain the target of 2 µm layer thickness, the whole sequence, including crystallization has to be repeated 5 times.

High quality PZT layers can be achieved with this CSD tool with a typical layer thickness of 2 µm, a layer uniformity of ± 0.9 % and (001) orientation.
After poling the layers show a longitudinal response $d_{33,f}$ of around 120 pm/V. The breakdown field is around 500 kV/cm using a 1 Hz test ramp.

A newly developed process with 100 nm per coated layer achieves 400 nm per RTP cycle and permits therefore a throughput of 3.2 wafer/h*µm (53 nm/min) for a total layer thickness target of 2µm for the actual tool configuration. An up scaling of the PTZ tool to the tool platform MC 208 CSD with a robot that runs on a linear unit in the tool centre, the throughput can easily be increased to 6.4 wafers/h*µm.

Public introduction[1]

[1] According to Deliverables list in Annex I, all restricted (RE) deliverables will contain an introduction that will be made public through the project WEBsite

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1.1 CSD Coating tool architecture

1.1.1 General

The Solar-Semi CSD (coating spin deposition) tool MC204 CSD was originally developed for resist coating applications in the semiconductor and MEMS industry. This tool has proven its industrial reliability with more than 50 installations. It consists of a basic platform with a central robot for wafer handling, a carrier loading unit, the coater system, a hotplate stack, including a cool plate and a transfer station to an RTP (Rapid Thermal Processing) furnace. Furthermore a second transfer robot permits to move wafers to the RTP oven, dogged onto the basic platform.
The cluster housing was equipped with a FFU (filter fan unit) on top and completely sealed to protect operators against toxic vapours.

Figure 1: MC 204 CSD Tool; (left) Tool Layout. (right) Picture while the assembly phase

In a typical process sequence wafers will be moved to the coating system to obtain a PZT layer by spinning on a liquid precursor and is then transferred to the hotplate for pyrolysis. This sequence of spin on, hotplate pyrolysis will be performed 4 times to obtain a layer thickness of typically 400 nm, followed by a RTP step for layer crystallization. In order to obtain a target of 2 µm layer thickness, the whole sequence, including crystallization has to be repeated 5 times.

1.1.2 Coater

An important feature of the films produced by spin-coating is that their thickness is highly uniform across the wafer and can be precisely controlled through variation of process parameters like rotational speed, duration, viscosity and temperature just to name a few. This is one of the biggest advantages of CSD as homogeneity is crucial for narrow tolerances and high yield in serial production.
The coater shows the following features:

- Covered chuck (a cover that seals the wafer chuck while spinning) or open bowl depending on the process choices
- Maximum spin speed at 3000 rpm for covered chuck and 6000 rpm for open bowl with an acceleration ramp of 6000 rpm.

- Chamber rinse for the outer process chamber, to prevent spin off material from creating particles.
- One solvent line for wafer surface pre-wetting
- 3 independently programmable PZT precursor dispense lines with precision pumps to apply the PZT material on the wafer.
- Each line can have different Zr/Ti ratio to avoid the development of gradients during crystallization. This will increase $e_{31,f}$ performance to -17 C/m^2
- Dispense lines equipped with PTFE filters near the point of use to prevent particles on the PZT layers.
- Dispense nozzle parking position completely sealed to protect the precursor solution.
- EBR (edge bed removal) nozzle to rinse away higher coating thickness at the wafer edge.

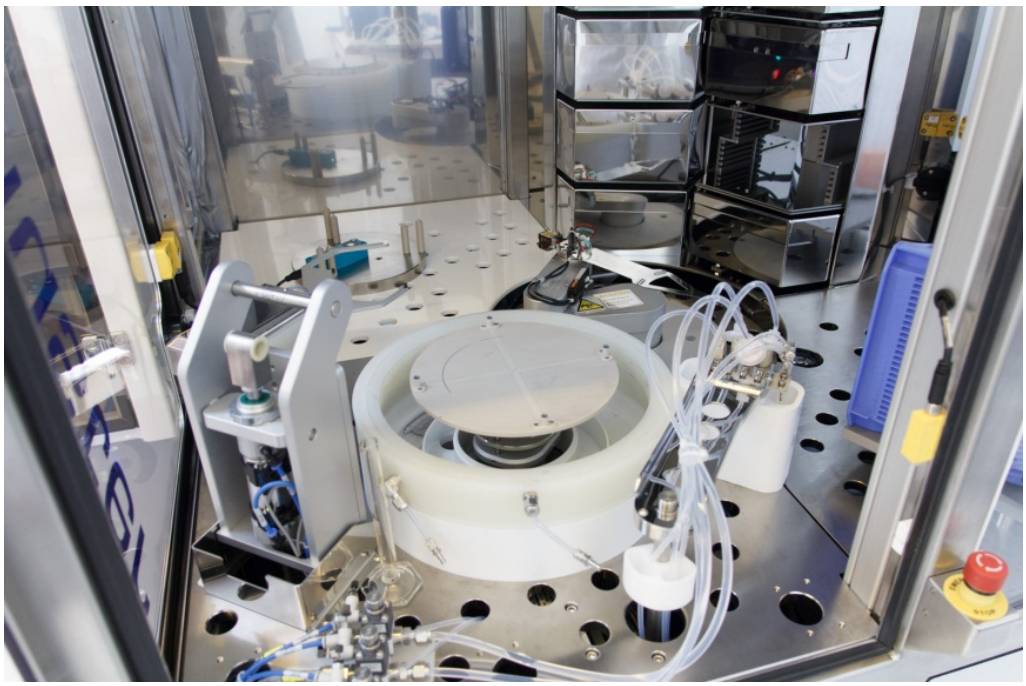


Figure 2: Coater bowl as open version with bowl rinse and process arm on the right with dispense lines

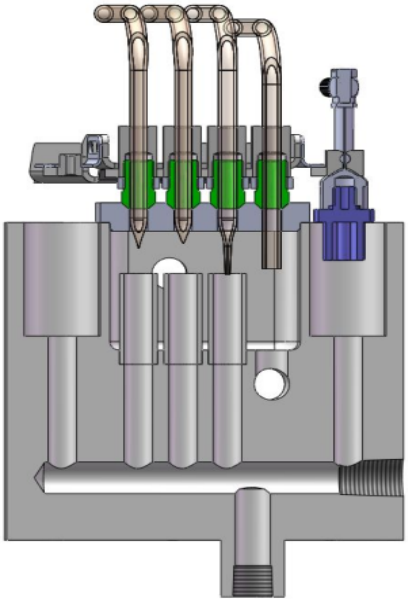


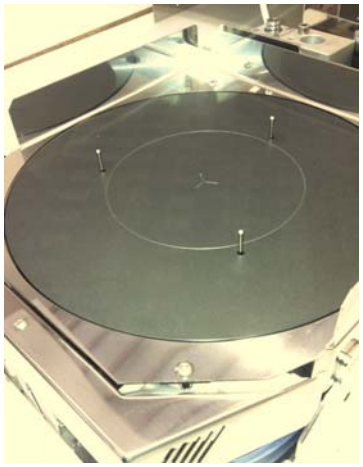
Figure 3 (left): Nozzle setup above the parking position; on the left the EBR nozzle; on top the filter; below the sealed parking bath where the nozzles drive in and stay protected.

1.1.3 Hotplate

In the next step the sol-gel transformation takes place, i.e. the solvent is removed followed by pyrolysis of the organic compounds, leaving an amorphous film. Both steps are carried out over a hotplate at elevated temperatures of up to 450°C.

The coater shows the following features:

- A maximum temperature with a uniformity of typically 1%
- Specially designed tips on the lifting pins for wafer edge handling
- Temperature ramp by programmable lifting pin speed
- N_2 inlet and exhaust to bring away all solvents and toxic gases



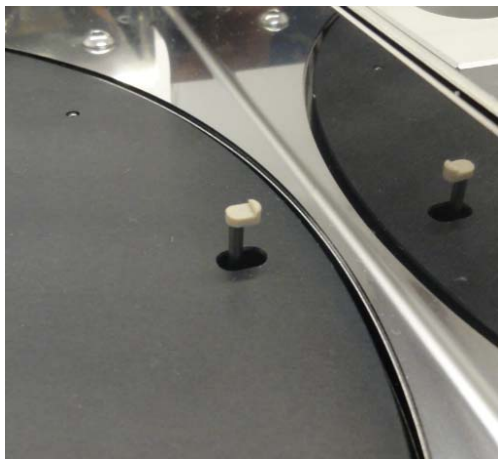


Figure 4: (left) Hotplate with cover opened up to see the pins lifted; (right) lift-pin tip design for edge handling.

It is desired that the wafer is heated to 350 °C during at least 10 s to avoid any thermal shock effects in the PZT coating. The programmed temperature ramp can be seen in Figure 5 that gives a nice 20 s ramp up to the pyrolysis temperature.

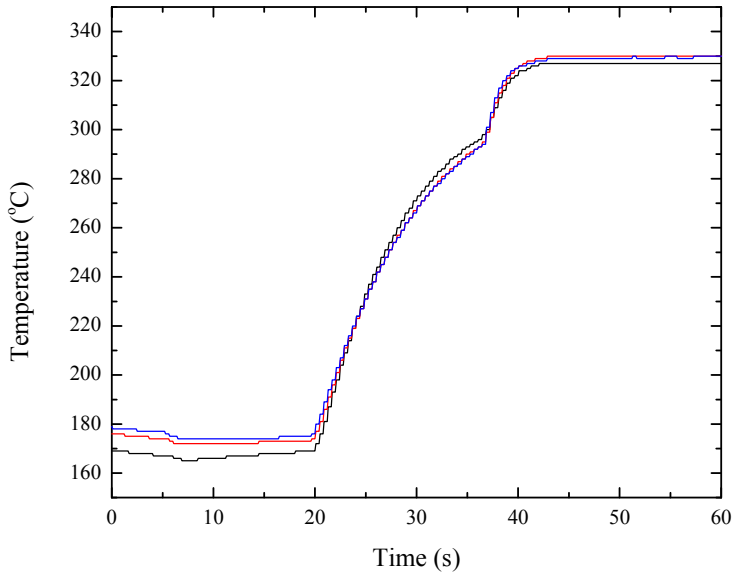


Figure 5: Heating profile achieved for the final program characterized using a TC wafer

1.1.4 RTP System

Upon completion of 4 PZT layers a temperature treatment follows, in which the initially amorphous coating is converted to a crystallographic arrangement, giving the film the intended piezoelectric properties. This transformation occurs at typically 550 °C to 650 °C and requires a dedicated furnace. In order to maximize throughput and to keep the thermal history at a minimum, heating and cooling cycles are kept as short as possible. The expression RTP (Rapid Thermal Processing) for this type of furnace reflects the fact, that the temperature can be raised during warm-up at a rate of up to 40 K per second. Of similar importance as the layer homogeneity in the deposition of the precursor solution is a uniform temperature distribution during crystallization for the quality of the final product. This requirement is almost perfectly met by the selected furnace as the measured temperature uniformity is better than ± 1 % at 700°C over a 200 mm wafer.

The RTP shows the following features:

- Top Load for automated robot loading
- Independent programming of top and bottom heating
- Individual lamp control for temperature uniformity fine tuning
- 2 gas control units (one for O_2 process gas; one for N_2 down-cooling)
- Quartz wafer carrier, compatible for 150 and 200 mm wafer
- Sacrificial quartz plate on top of the wafer for PbO absorption
- Modified Gas inlet for optimum gas-flow on the wafer surface
- In situ temperature measurement via TC (Thermo Couple)

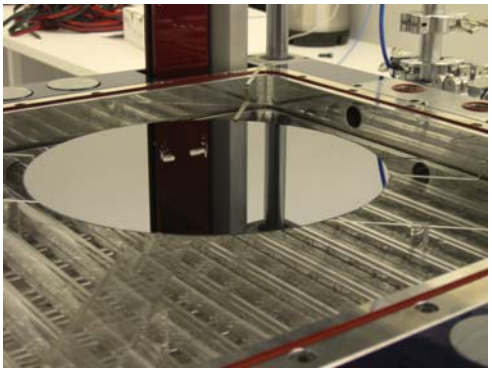


Figure 6: (left) RTP furnace opened; lower lamp array can be seen. (right) quartz carrier with 200 mm wafer; the carrier can also hold the sacrificial plate (not mounted)

Location	Meas. #1	Meas. #2
0° / 50mm	691.9	699.8
90° / 50mm	694.3	701.0
180° / 50mm	693.8	700.4
270° / 50mm	696.2	702.4
45° / 95mm	687.7	695.6
135° / 95mm	685.8	694.4
225° / 95mm	687.1	694.5
315° / 95mm	692.8	698.6

	#1 T [°C]	#2 T [°C]
Max	696.2	702.4
Min	685.8	694.4
Average	691.2	698.3
Max-Min	10.4	8.0
Limit	14 (± 7)	14 (± 7)
Result	**OK**	**OK**

Temperature uniformity of RTP furnace across 200 mm wafer

Table 1: Temperature uniformity is in the worst case +/- 0,8 %

2 MATERIAL PERFORMANCE

2.1 Thickness uniformity

High quality PZT layers can be achieved with this CSD tool with a typical layer thickness of 2 µm, a layer uniformity of ± 0.9 % and a (001) orientation. After poling the layers show a longitudinal response $d_{33,f}$ of around 120 pm/V.

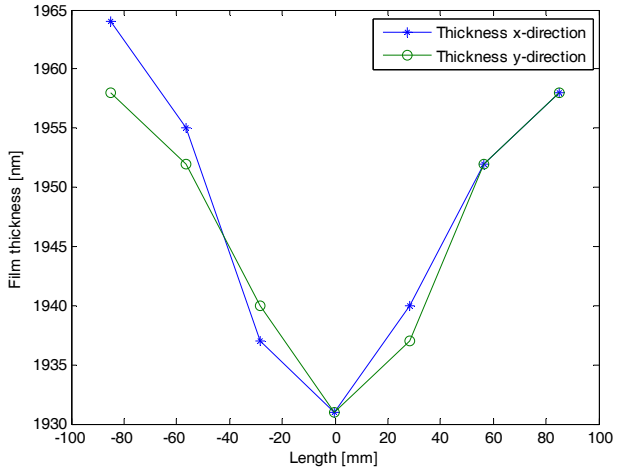
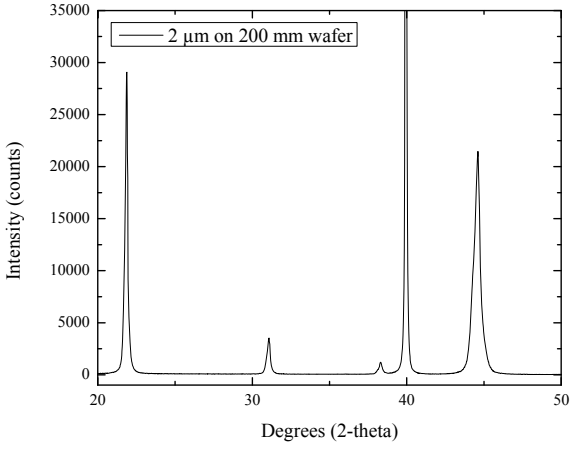


Figure 7: Layer uniformity wafer mapping on a 200 mm wafer; measured by ellipsometry

2.2 Crystallographic quality

XRD analysis of a 2 µm film on 200 mm in **Error! Reference source not found.** show that the PZT film is highly (001) oriented. Using a PZT powder as reference the film is 95,7 % (001) oriented which is very encouraging.



Firgure 8: X-ray diffractogram of the center area of a 200 mm wafer with 2 µm PZT

2.3 Ferro and piezoelectric properties

A typical ferroelectric hysteresis loop for a standard 2 µm PZT (001) film deposited on a 200 mm platinized wafer is shown in shown in Figure 9 (green). The film exhibits a maximum polarization of

approximately 30 µC/cm2 @ 125 kV/cm and a remanent polarization of 15 µC/cm^2. A coercive field of about 30kV/cm is achieved. The second graph (blue) displays the large signal displacement in longitudinal direction during AC voltage application. From the data a $d_{33,f}$ value of approximately 120 pm/V can be estimated for the large signal actuation. CSD PZT displays a general $e_{31,f}$ of -15 C/cm^2 at zero bias.

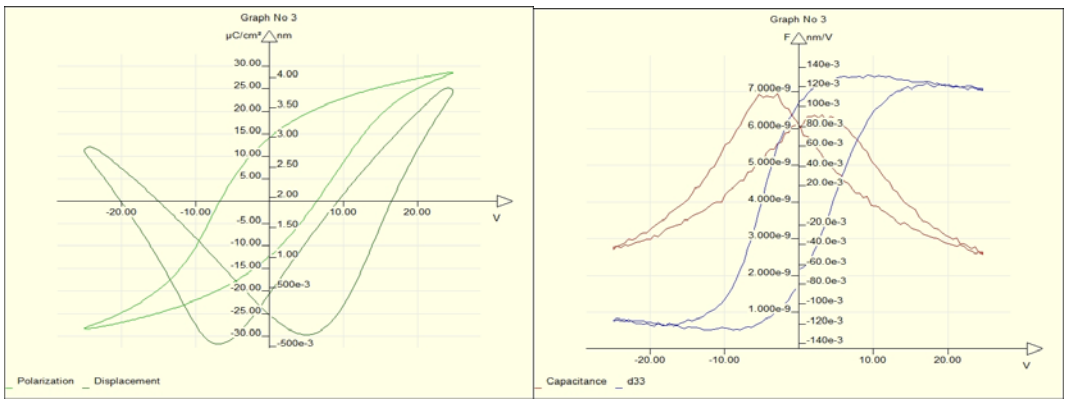


Figure 9: Small signal and large signal material properties of PZT CSD thin films

2.4 Breakdown field

The breakdown voltage was found to be 460 kV/cm using a triangular test ramp of 1 Hz on a 0,125 mm^2 pad as shown in Figure 10:

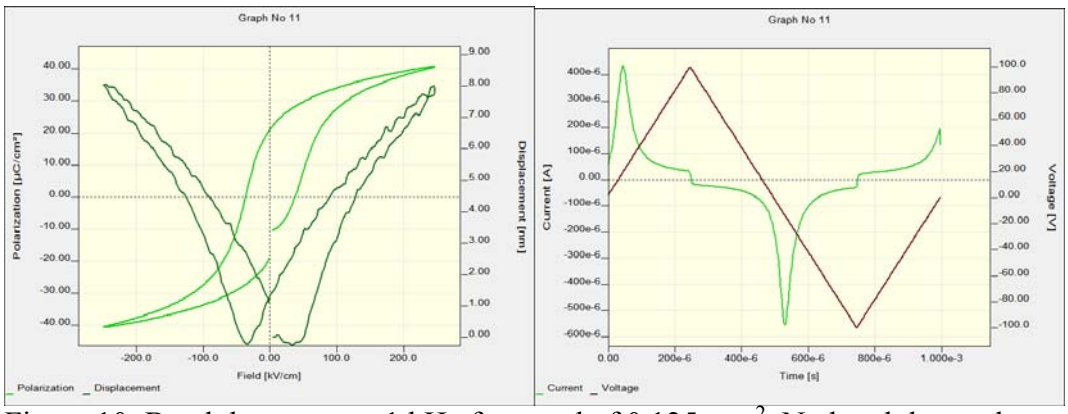


Figure 10: Breakdown test at 1 kHz for a pad of 0,125 mm^2. No breakdown observed up to 500 kV/cm.

2.5 Productivity

The newly developed process with 100 nm per coated layer achieves 400 nm per RTP cycle and permits therefore a throughput of 3.2 wafer/h*µm (53 nm/min) for a total layer thickness target of 2µm for the actual tool configuration. An up scaling of the PTZ tool to the tool platform MC 208 CSD with a robot that runs on a linear unit in the tool centre, the throughput can easily be increased to 6.4 wafer/h*µm (106 nm/min). Thicknesses from 100 nm to 4µm can be realized.

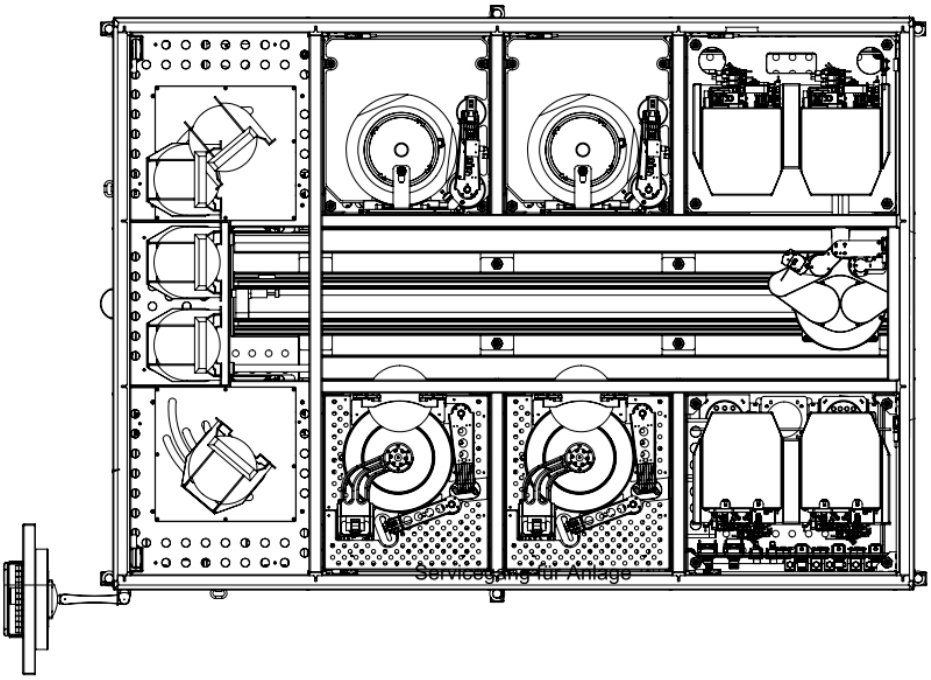


Figure 11: Tool layout of the MC 208 CSD for throughputs of 6.4 wafers/h*µm